

FIG. 1  
PRIOR ART

10

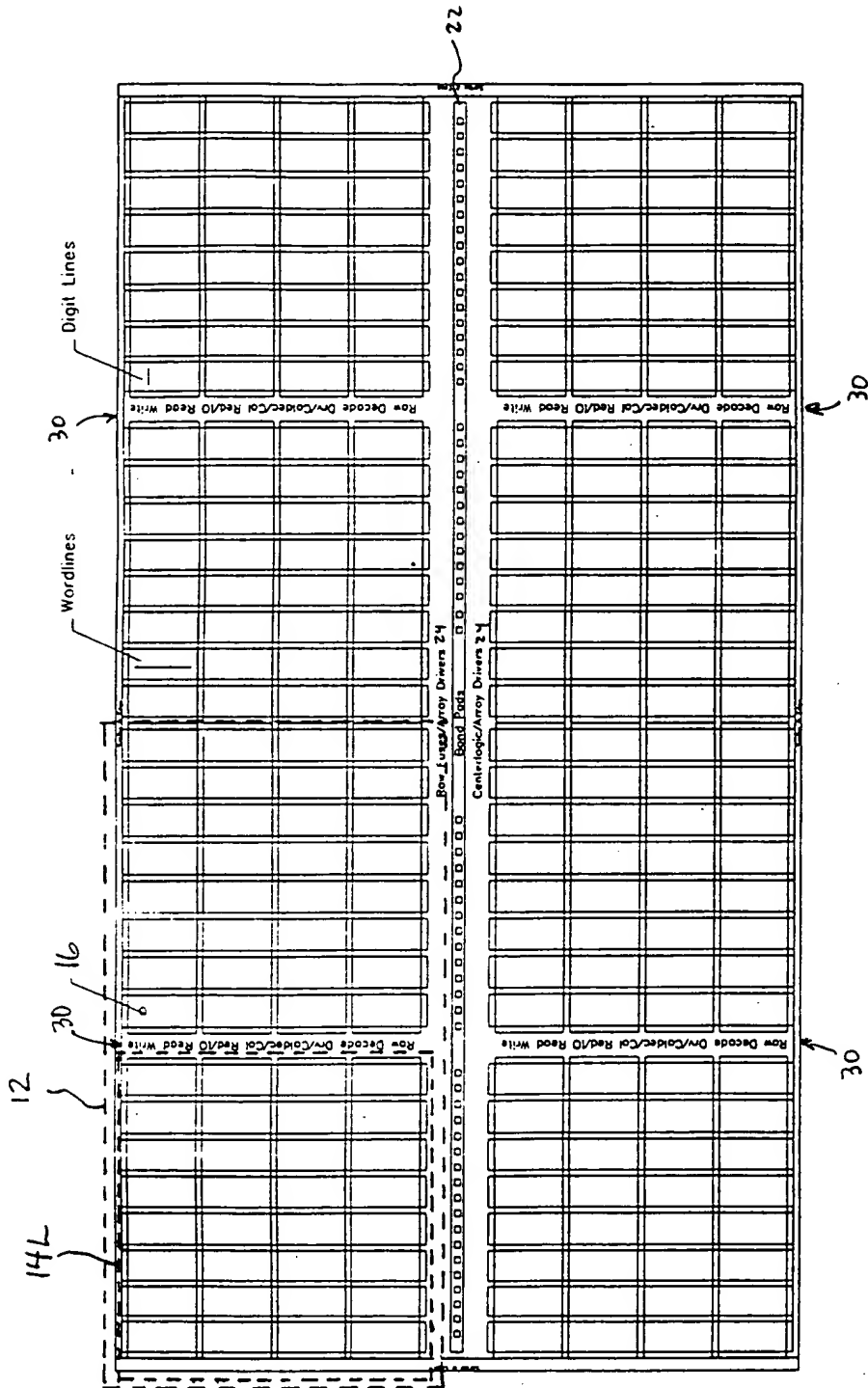


FIGURE 2

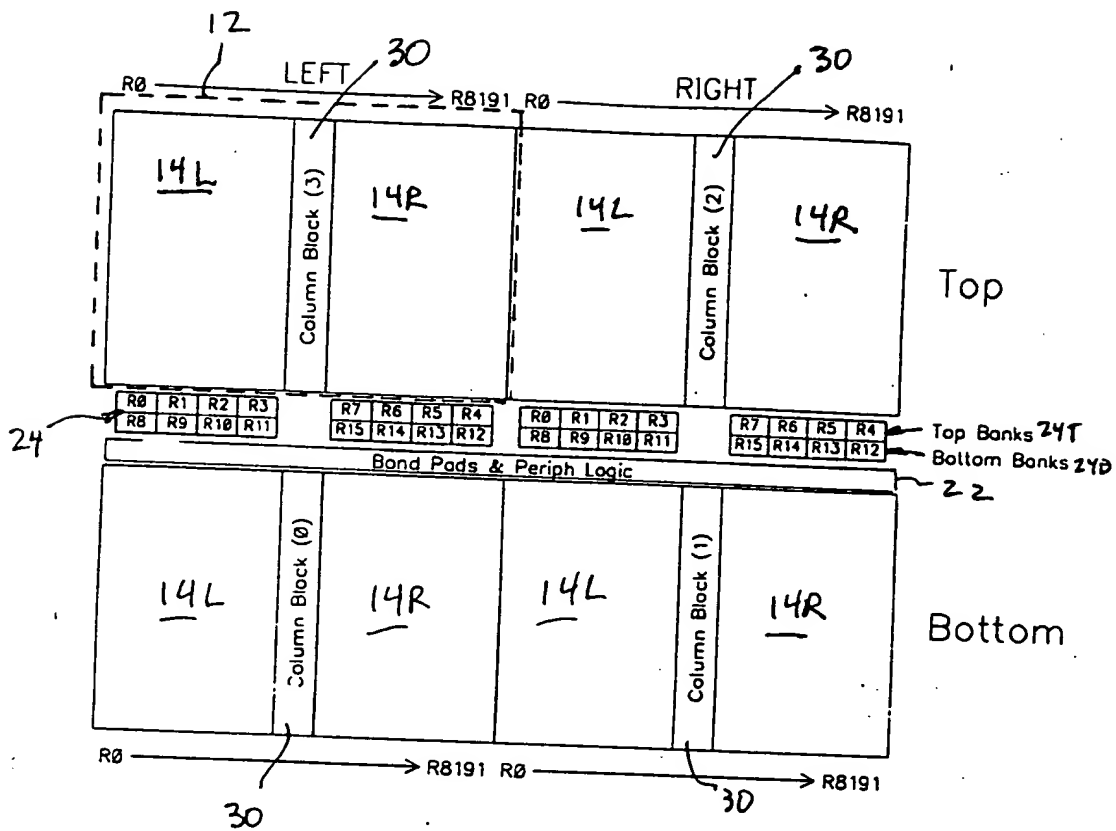


FIGURE 3

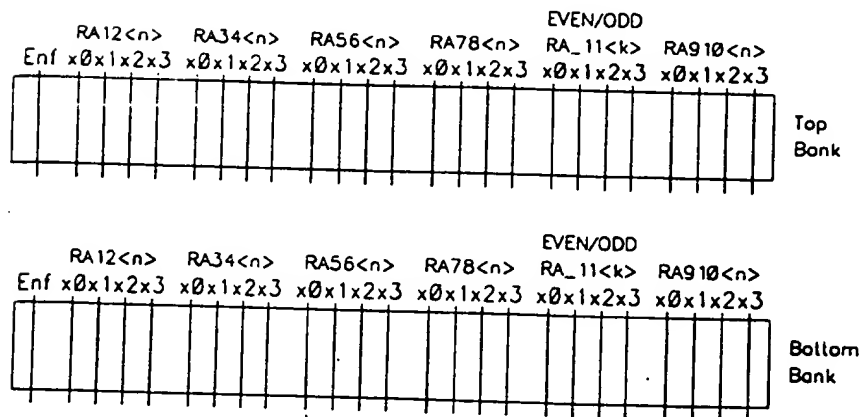


FIGURE 4

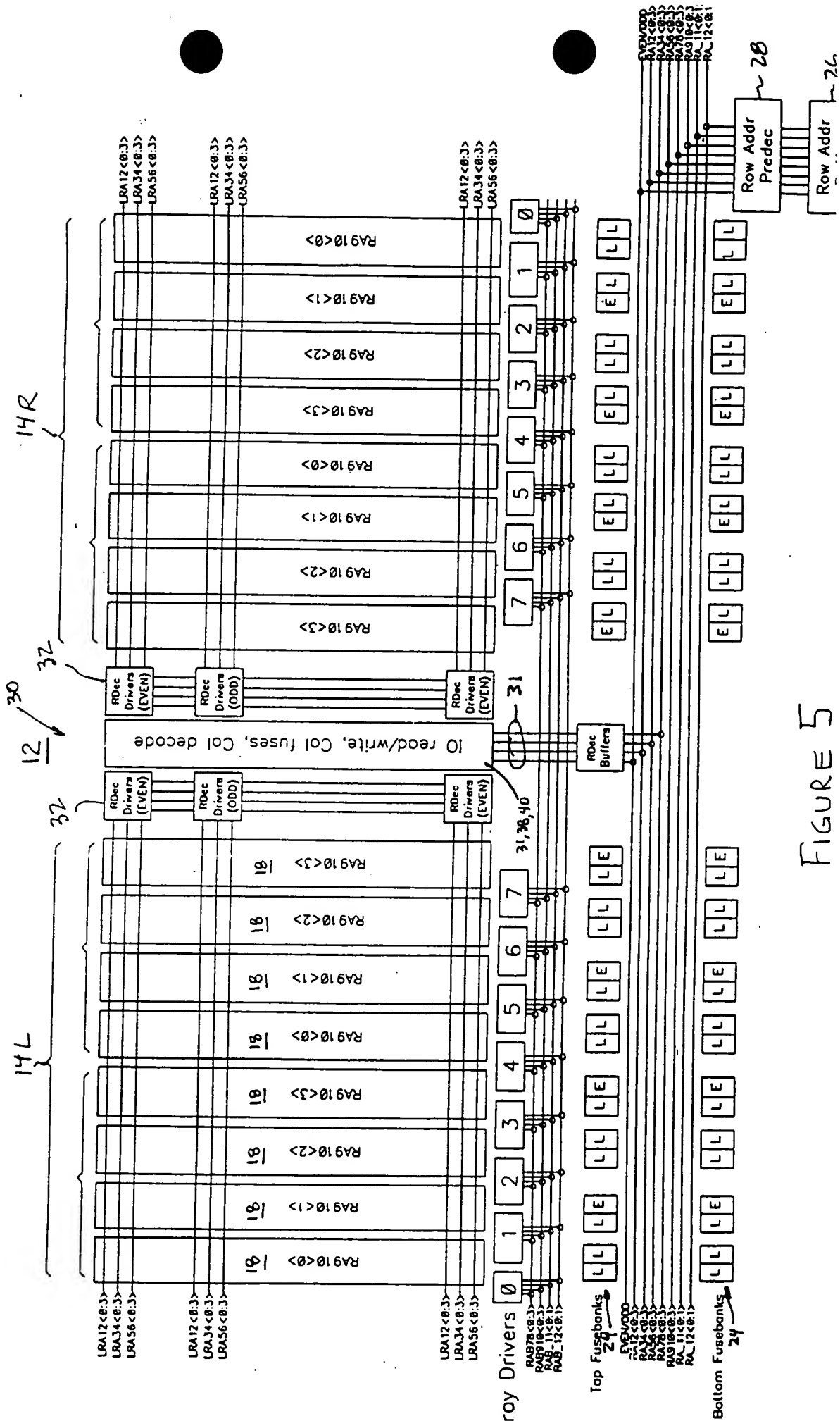


FIGURE 5



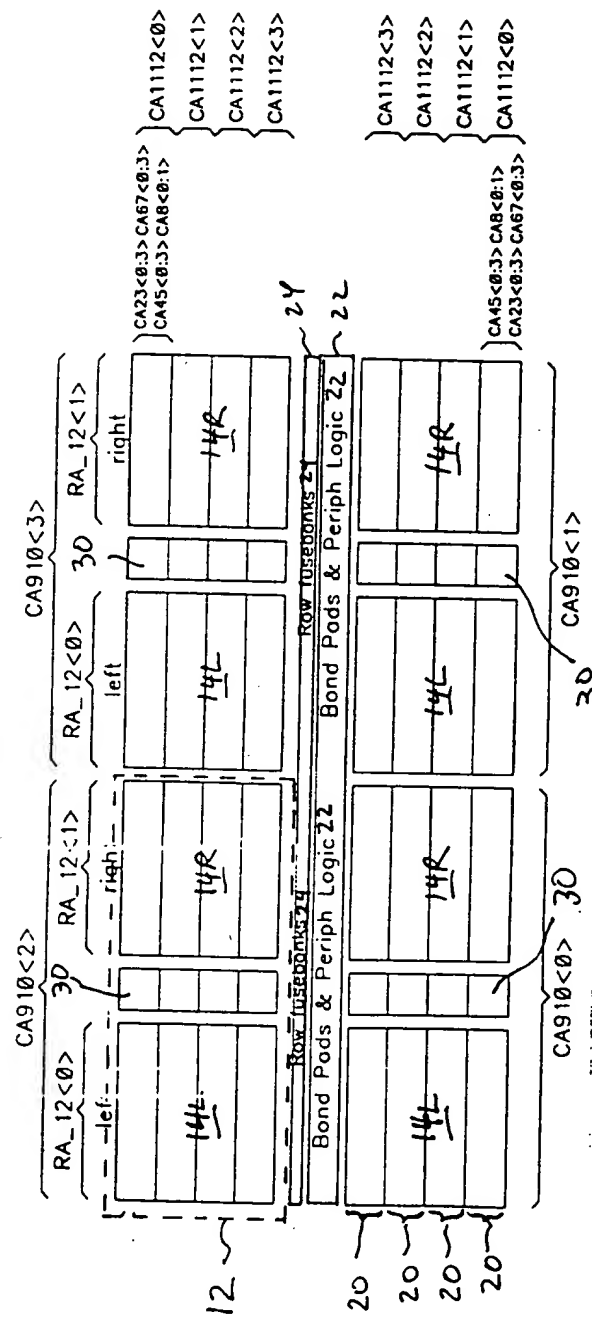


FIGURE 6

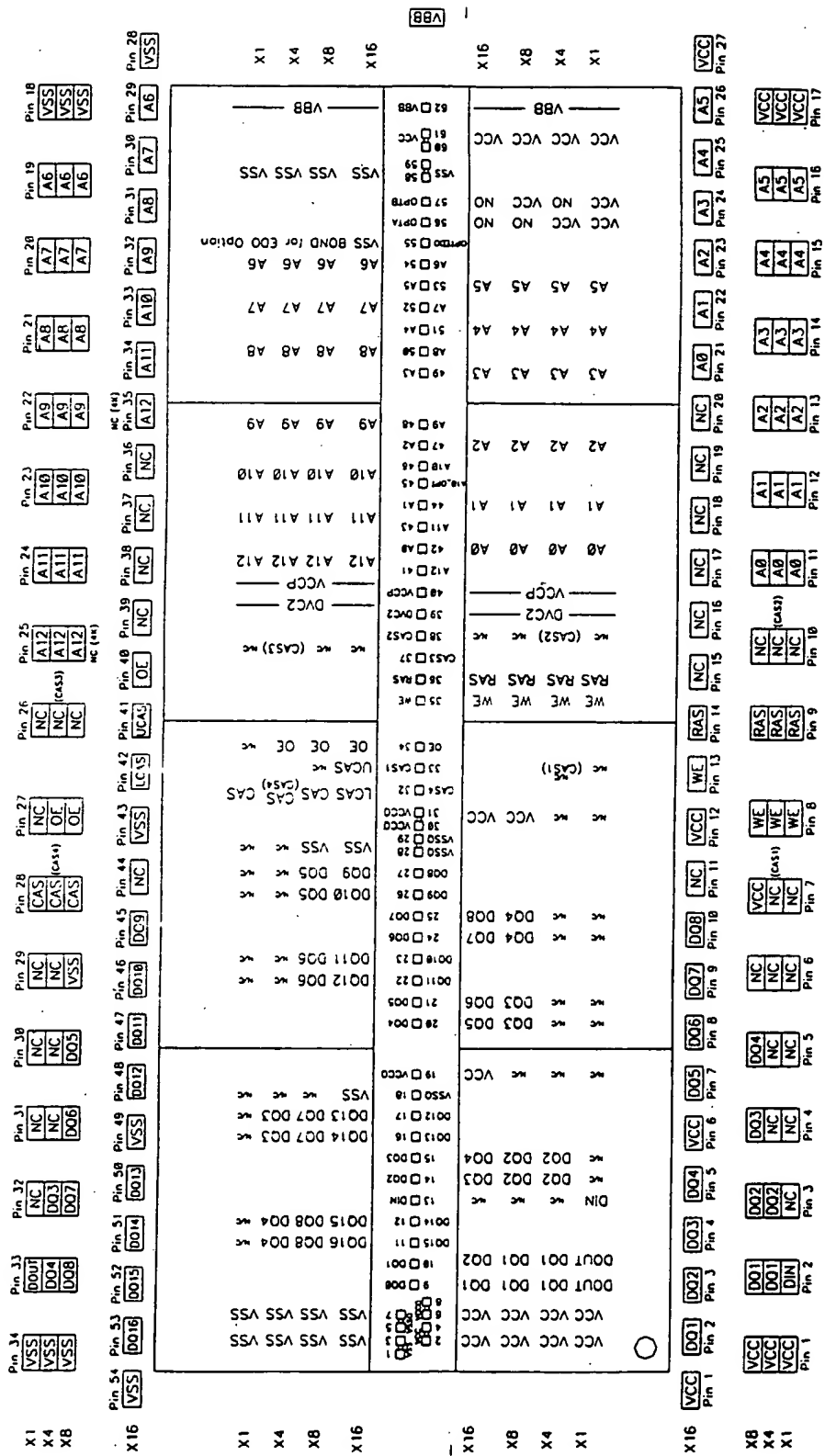


FIGURE 7

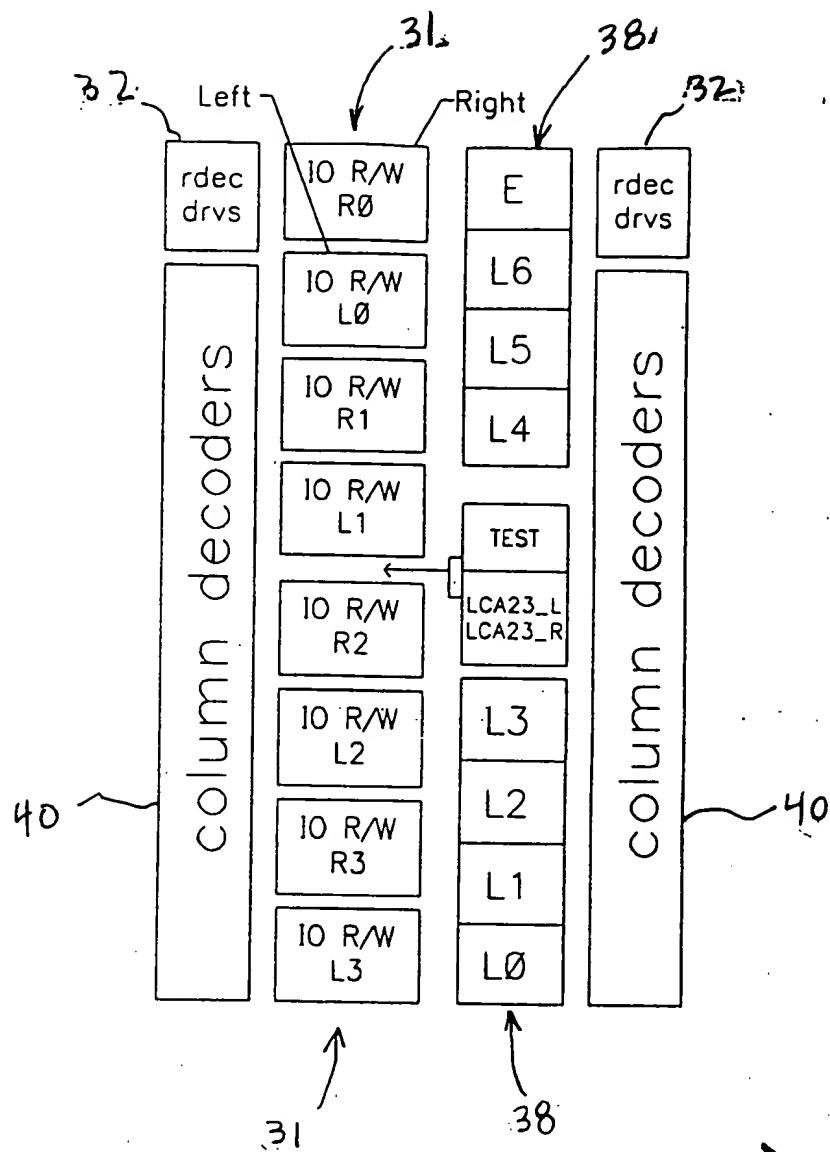


FIGURE 8

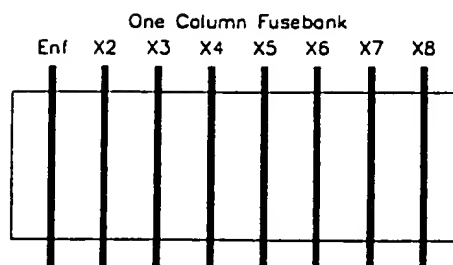


FIGURE 10

# Row Redundant Laser Fuses

Row Predec Addr	Blow Laser Fuse			
RA12<0>	x0	x1	x2	x3
RA12<1>	x0	x1	x2	x3
RA12<2>	x0	x1	x2	x3
RA12<3>	x0	x1	x2	x3
RA34<0>	x0	x1	x2	x3
RA34<1>	x0	x1	x2	x3
RA34<2>	x0	x1	x2	x3
RA34<3>	x0	x1	x2	x3
RA56<0>	x0	x1	x2	x3
RA56<1>	x0	x1	x2	x3
RA56<2>	x0	x1	x2	x3
RA56<3>	x0	x1	x2	x3
RA78<0>	x0	x1	x2	x3
RA78<1>	x0	x1	x2	x3
RA78<2>	x0	x1	x2	x3
RA78<3>	x0	x1	x2	x3
EVEN	x0	x1	x2	x3
ODD	x0	x1	x2	x3
RA_11<0>	x0	x1	x2	x3
RA_11<1>	x0	x1	x2	x3
RA910<0>	x0	x1	x2	x3
RA910<1>	x0	x1	x2	x3
RA910<2>	x0	x1	x2	x3
RA910<3>	x0	x1	x2	x3

Note: Boxed fuses are the 'blown' fuses.

Pretest Address  
(compressed to 8meg block;  
unscrambled addresses)

BLOCK	ROW Addresses	
R0 R8	4,5,6,7	
R1 R9	1016,1017,1018,1019	
R2 R10	1028,1029,1030,1031	
R3 R11	2040,2041,2042,2043	
R4 R12	2052,2053,2054,2055	
R5 R13	3064,3065,3066,3067	
R6 R14	3076,3077,3078,3079	
R7 R15	4088,4089,4090,4091	

FIGURE 11

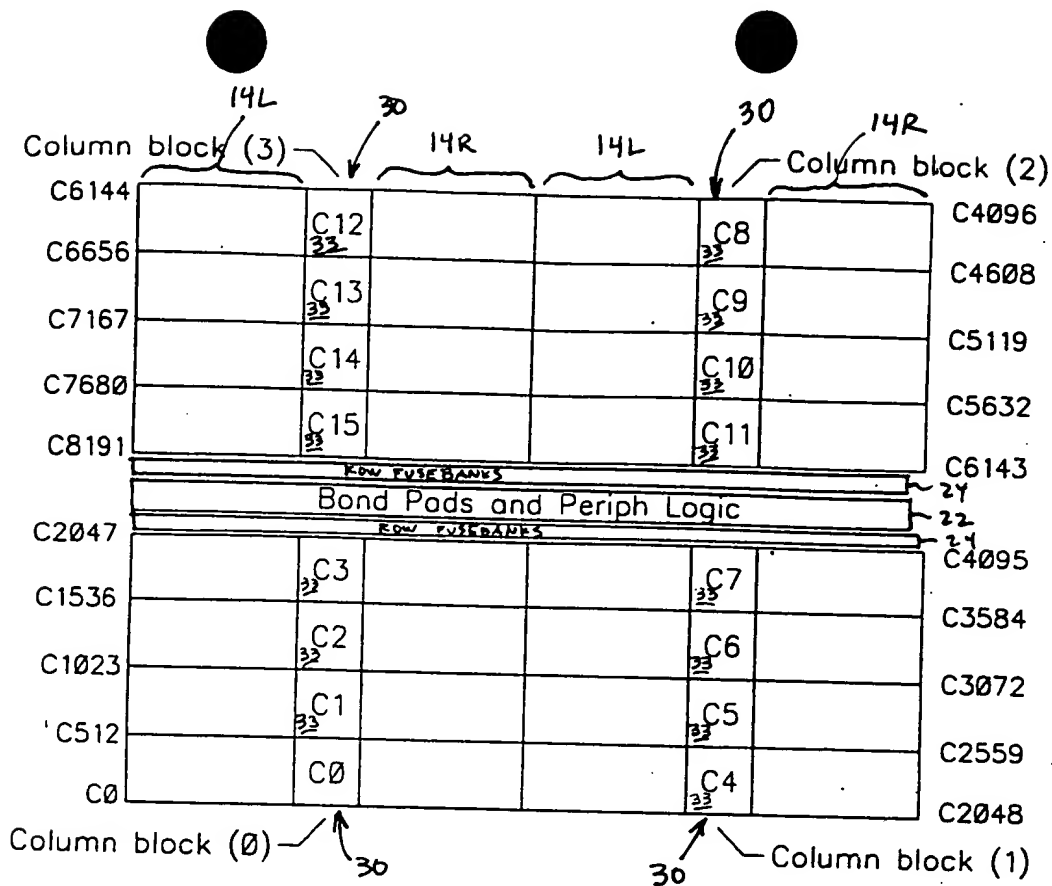


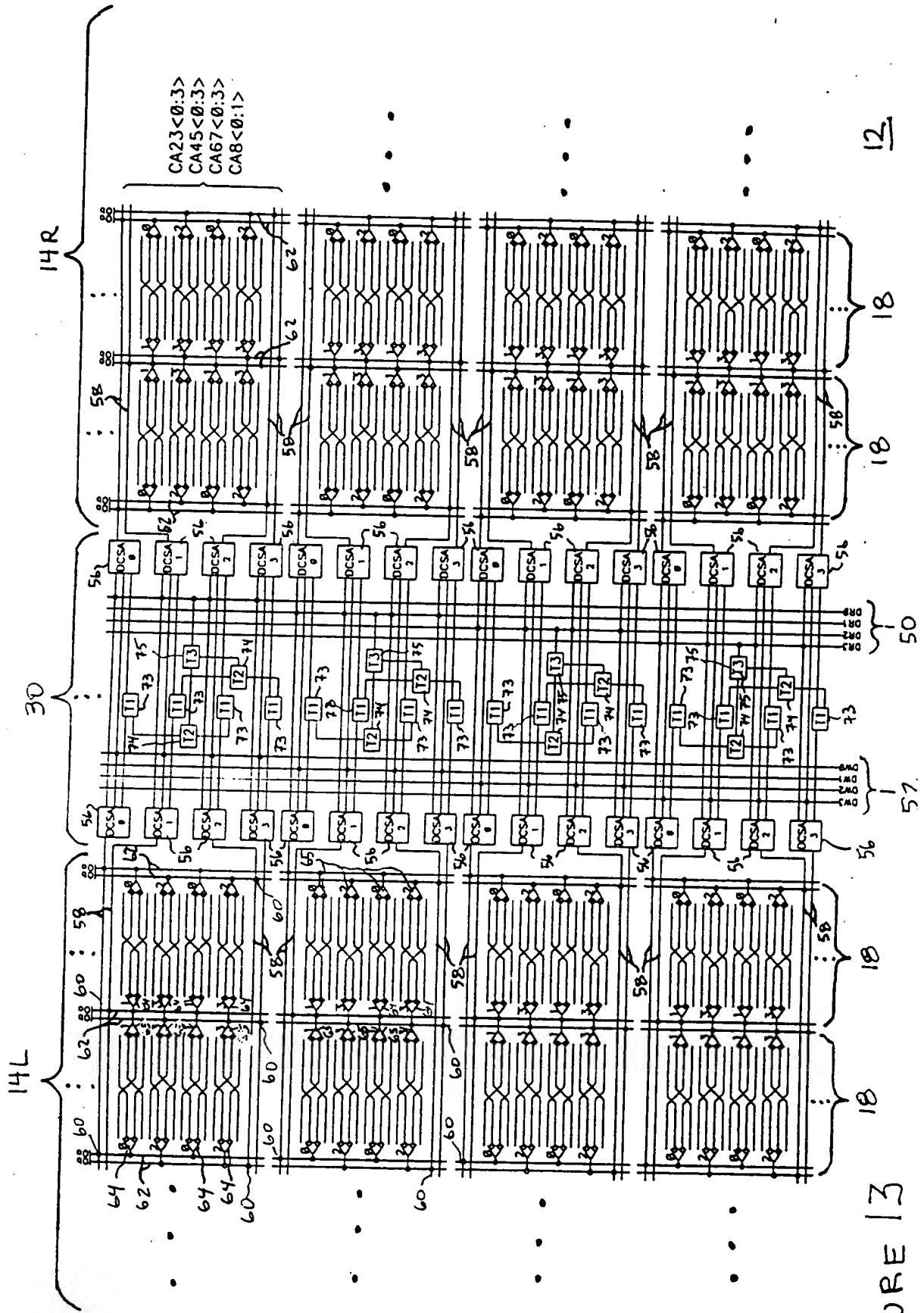
FIGURE 9

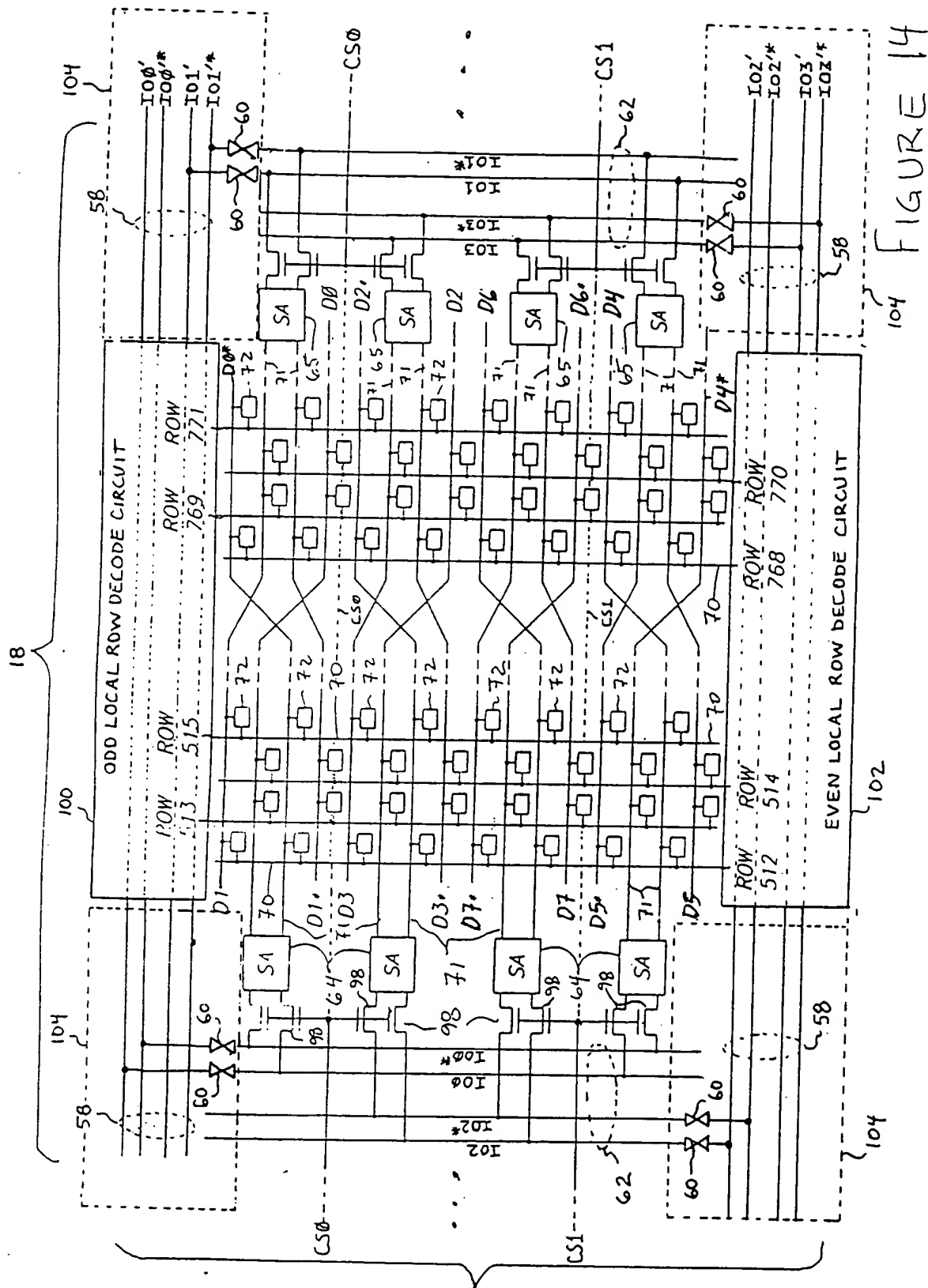
## Column Redundant Laser Fuses

Col Predec Addr	Blow Laser Fuse
CA23<0>	NONE
CA23<1>	X2
CA23<2>	X3
CA23<3>	X2, X3
CA45<0>	NONE
CA45<1>	X4
CA45<2>	X5
CA45<3>	X4, X5
CA67<0>	NONE
CA67<1>	X6
CA67<2>	X7
CA67<3>	X6, X7
CAB<0>	NONE
CAB<1>	X8

Bank	Pre-test Address						
	A8	A7	A6	A5	A4	A3	A2
0	0	0	0	0	1	1	1
1	0	0	0	0	1	1	0
2	0	0	0	0	1	0	1
3	0	0	0	0	1	0	0
4	0	0	0	0	0	0	0
5	0	0	0	0	0	0	1
6	0	0	0	0	0	1	0
7	NA						

FIGURE 12





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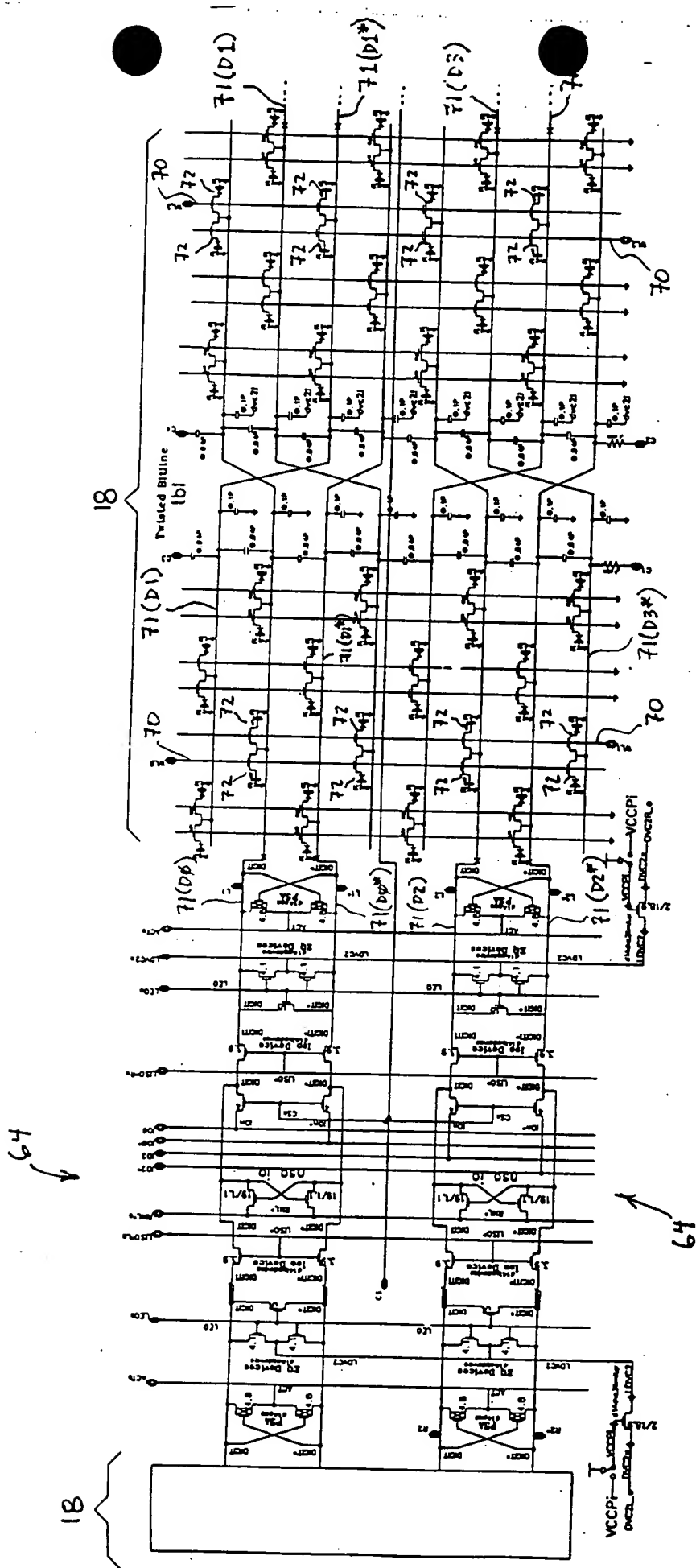


FIGURE 15



64

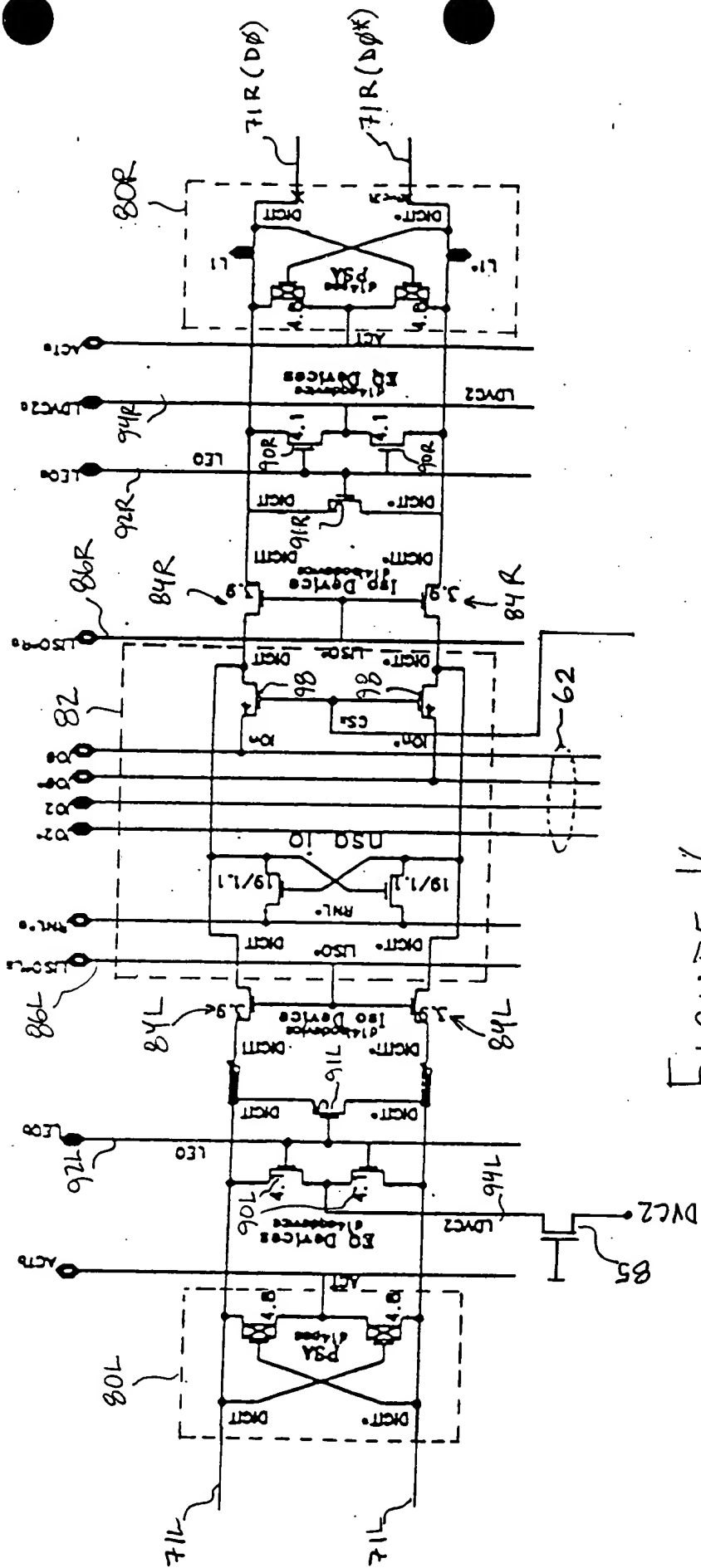


FIGURE 16

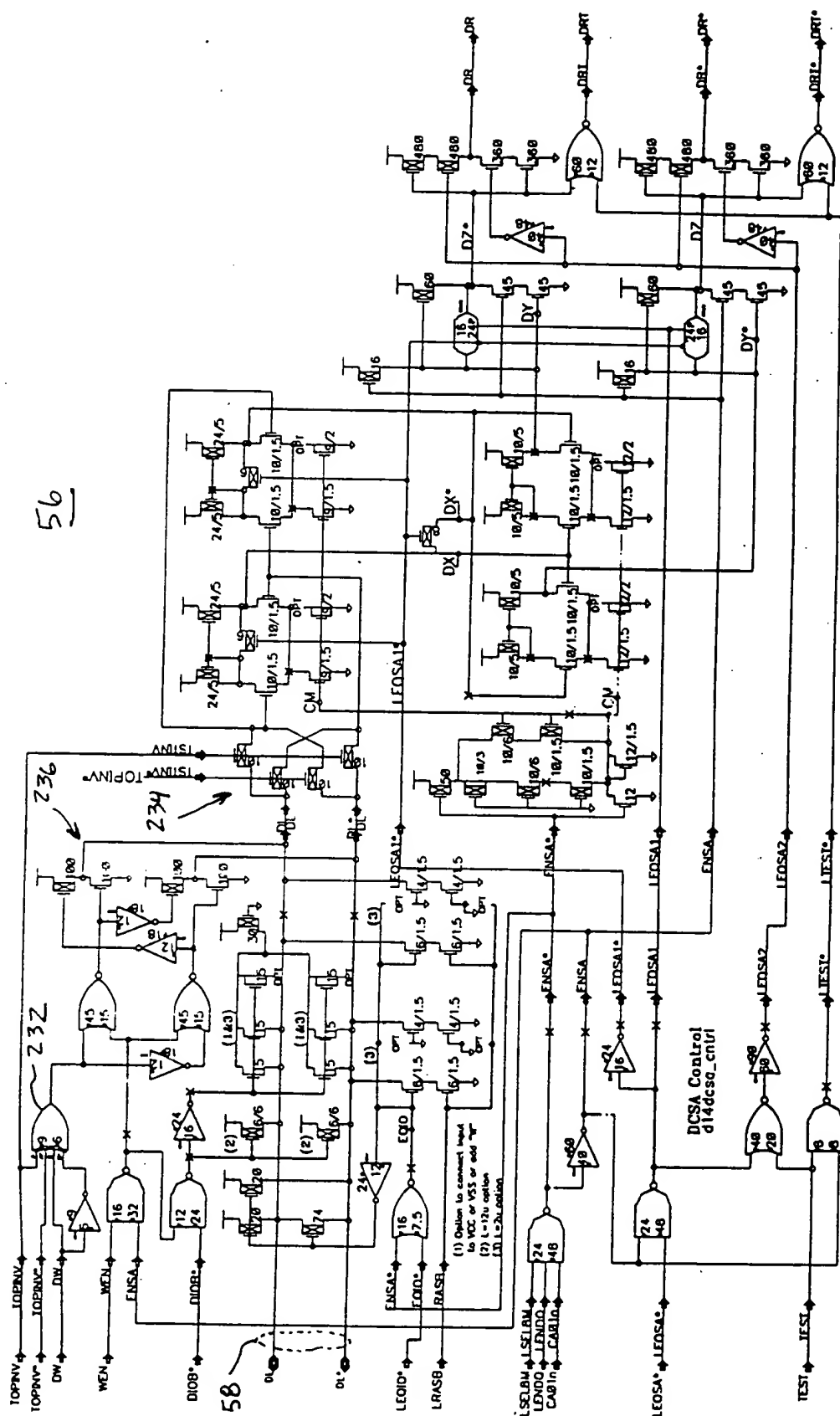


FIGURE 17

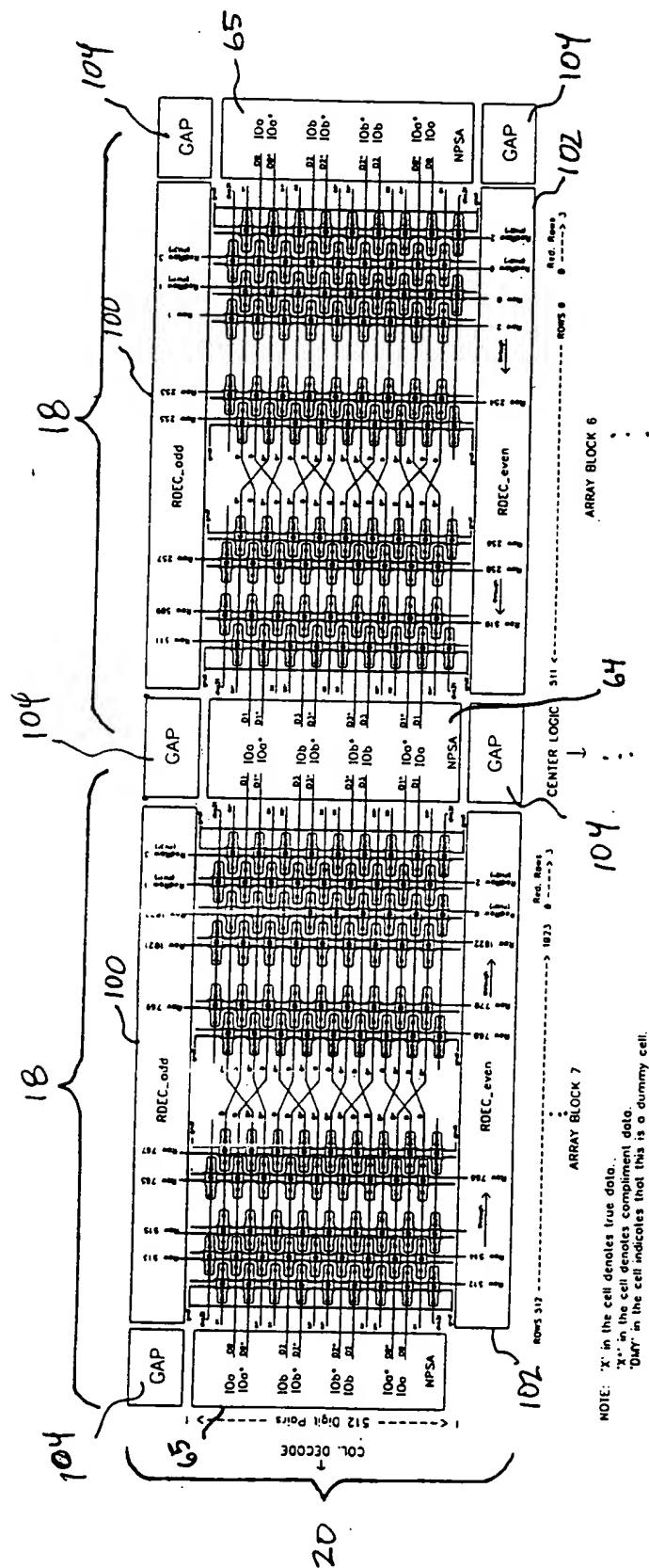


FIGURE 18

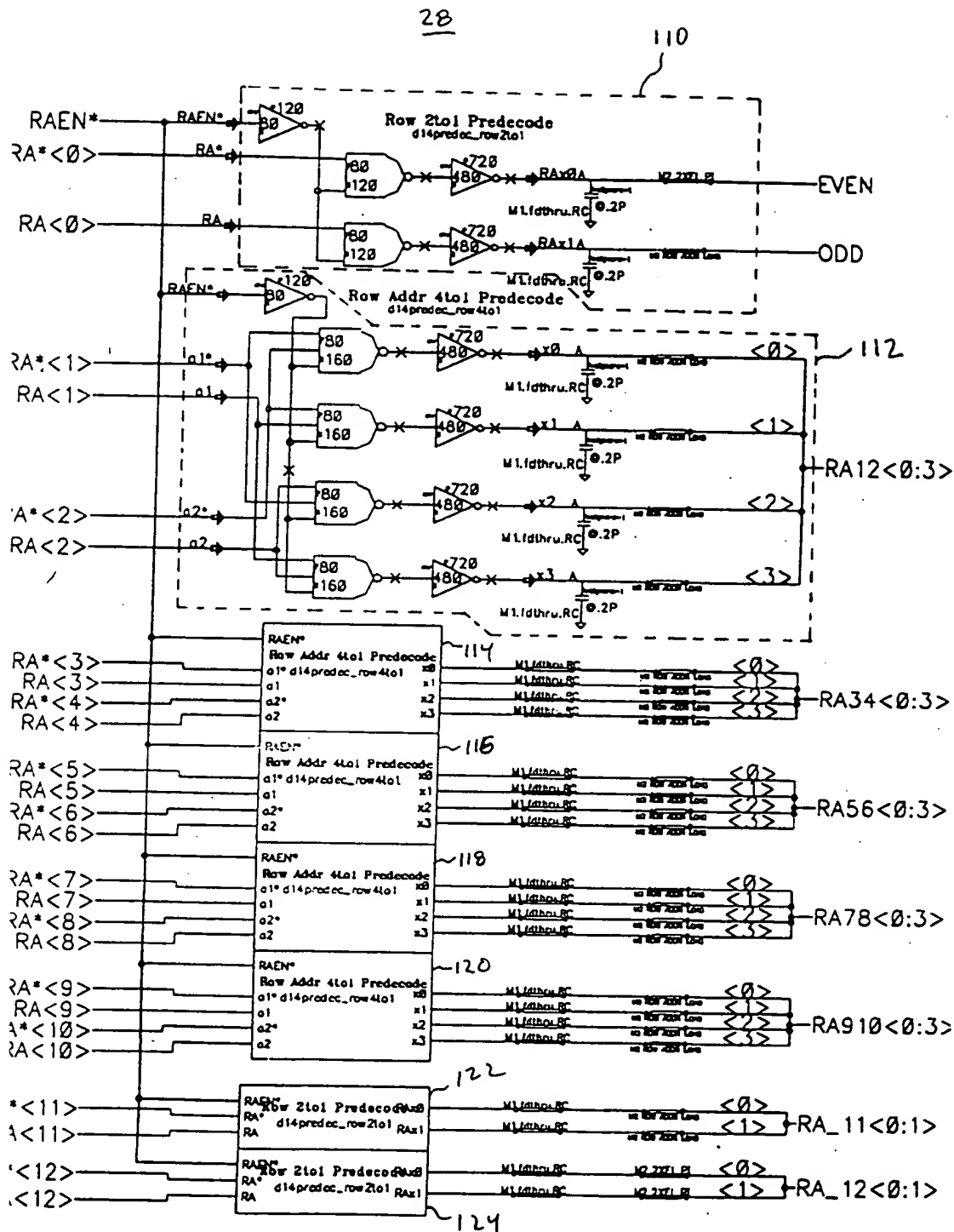


FIGURE 19

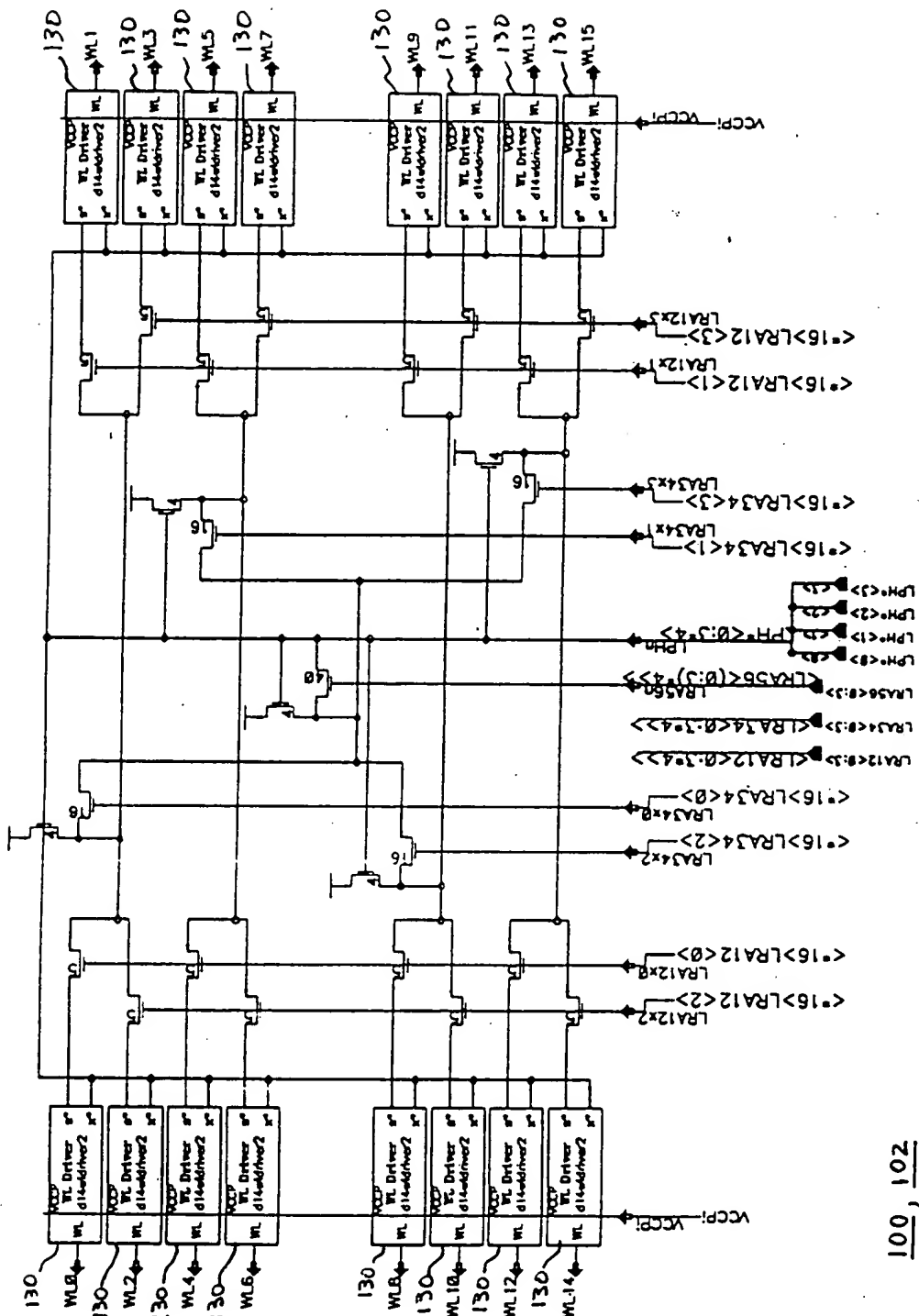


FIGURE 20

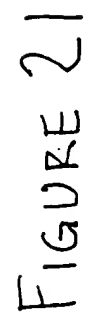


FIGURE 21

## Laser/Electrical Fuse Options

<b>OPT4KREF</b>		<b>COLRED</b>	
not blown	8K Refresh (default)	not blown	fast EQIO/EQSA (default)
blown	4K Refresh	blown	slow EQIO/EQSA
<b>OPTFAST</b>		<b>OPTSRB OPTSRA</b>	
not blown	slow (default)	not blown	not blown
blown	fast	blown	blown
<b>OPTS</b>		<b>Ref Rate</b>	
not blown	fast-page (default)	not blown	128ms (Default)
blown	static column	blown	192ms
<b>ROWRED</b>		blown	256ms
not blown	not used	blown	64ms
blown	not used	<b>ENTOPO</b>	
		not blown	data topo on (default)
		blown	data topo off

## Bonding Options

<b>XOPTA</b>	<b>XOPTB</b>	
NO	NO	OPTX16 (default)
NO	VCC	OPTX8
VCC	NO	OPTX4
VCC	VCC	OPTX1
<b>OPTEDO</b>		
NO		no EDO (default)
VSS		EDO

Option Fuse	Option Fuse Selection Address					
	A10	A9	A8	A7	A6	A5
OPT4KREF	1	1	1	0	0	0
OPTS	1	1	1	0	0	1
OPTFAST	1	1	1	0	1	0
ROWRED	1	1	1	0	1	1
COLRED	1	1	1	1	0	0
OPTSRA	1	1	1	1	0	1
OPTSRB	1	1	1	1	1	0
ENTOPO	1	1	1	1	1	1

FIGURE 22

# INPUTS OUTPUTS

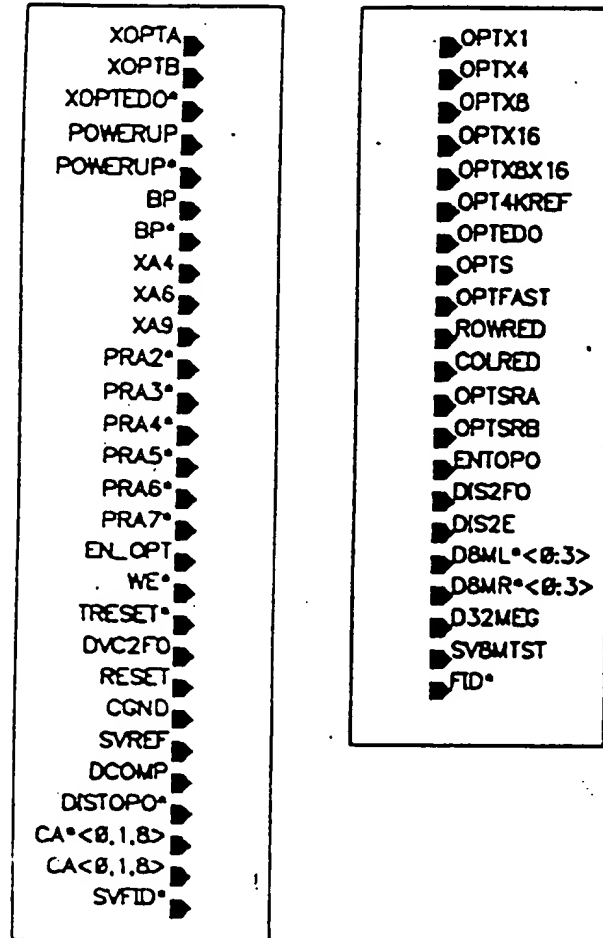


FIGURE 23



# 32MEG OPTION LOGIC

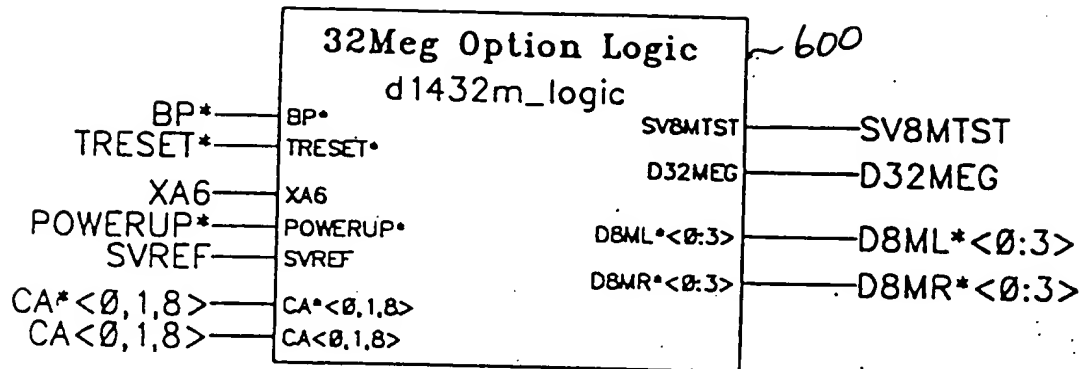


FIGURE 24

# BONDING OPTIONS

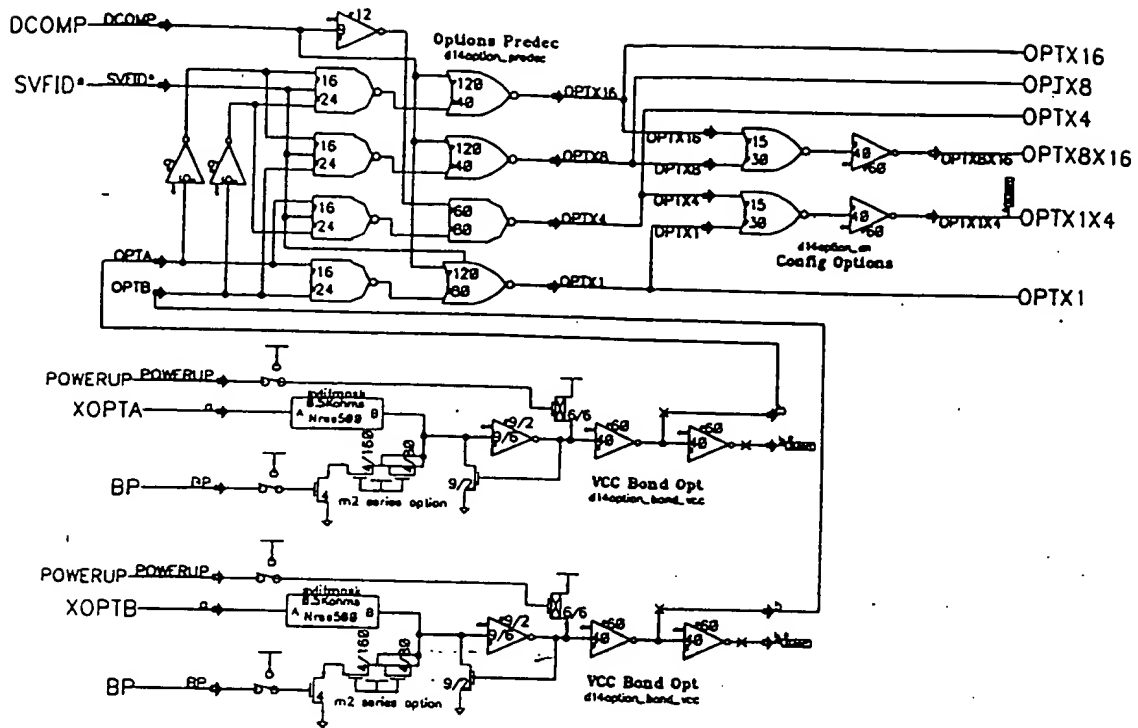


FIGURE 25

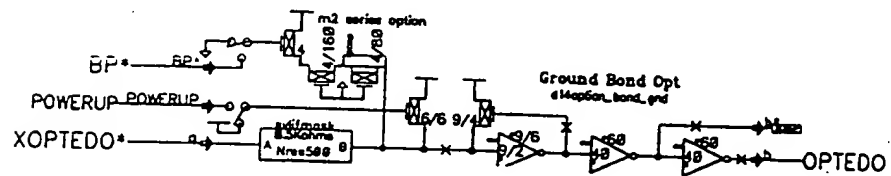


FIGURE 26

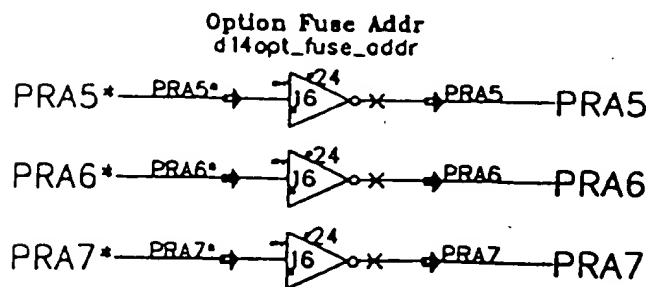


FIGURE 77

# LASER FUSE I.D. ADDRESS

(X3)

613

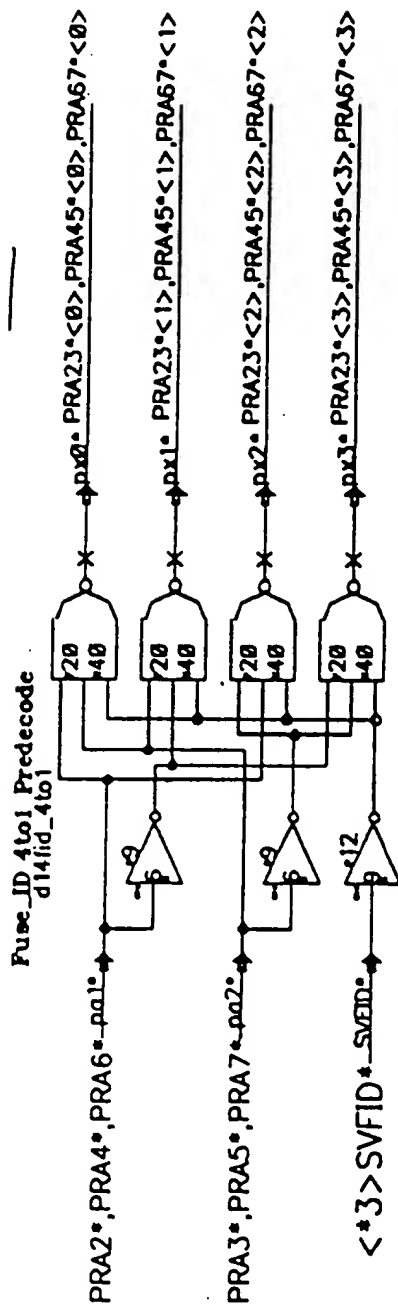


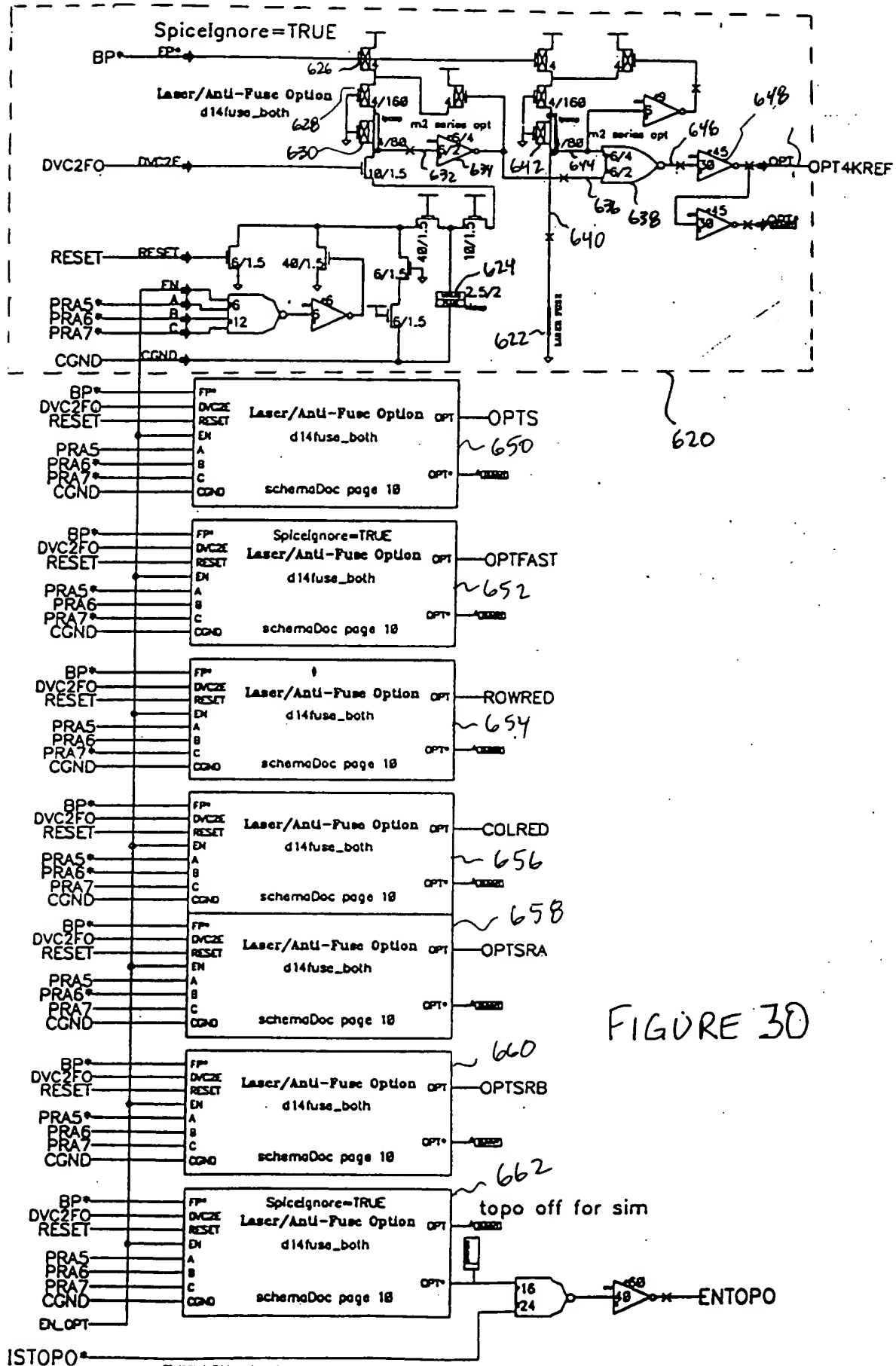
FIGURE 28

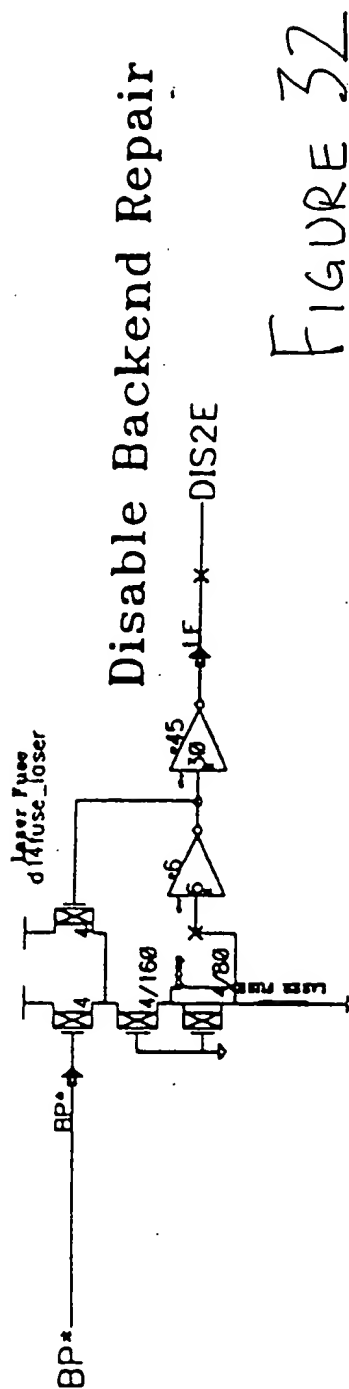
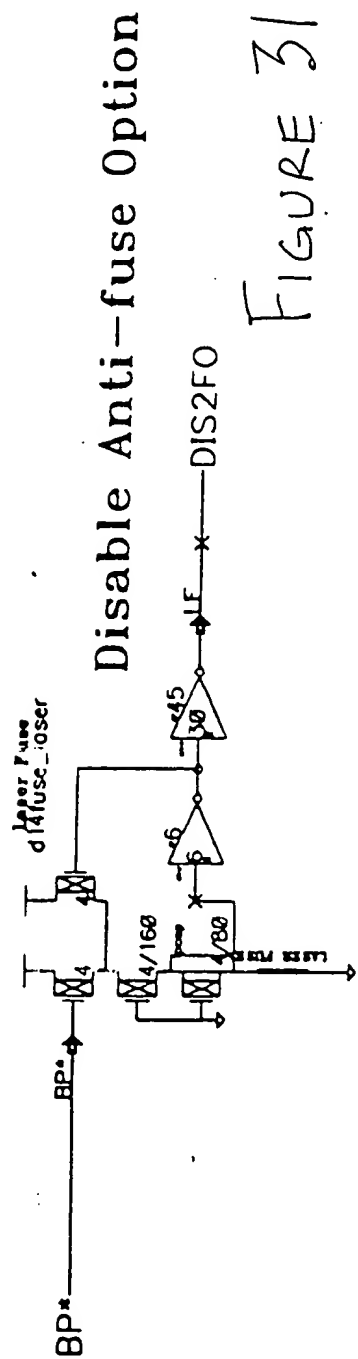
[illegible]

**Fuse Blown = Logic "1"**

FIGURE 29

# LASER/ELECT FUSE OPTIONS





# INPUTS      OUTPUTS

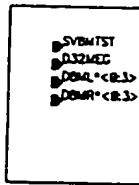
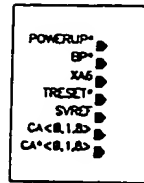


FIGURE 34

## 8Meg Array ICC—standby test

A1	A8	A7	Signal De-activated	Array Section Enabled (Ref to X4)
0	0	0	D8ML*<0>	LEFT DQ0
0	0	1	D8MR*<0>	RIGHT DQ0
0	1	0	D8ML*<1>	LEFT DQ1
0	1	1	D8MR*<1>	RIGHT DQ1
1	0	0	D8ML*<2>	LEFT DQ2
1	0	1	D8MR*<2>	RIGHT DQ2
1	1	0	D8ML*<3>	LEFT DQ3
1	1	1	D8MR*<3>	RIGHT DQ3

FIGURE 33

# XA6 Supervoltage Detect/Latch 600

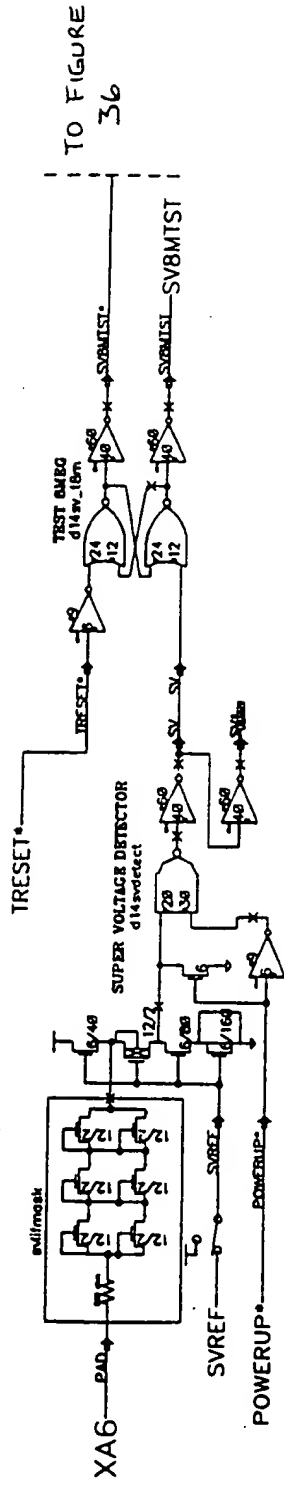


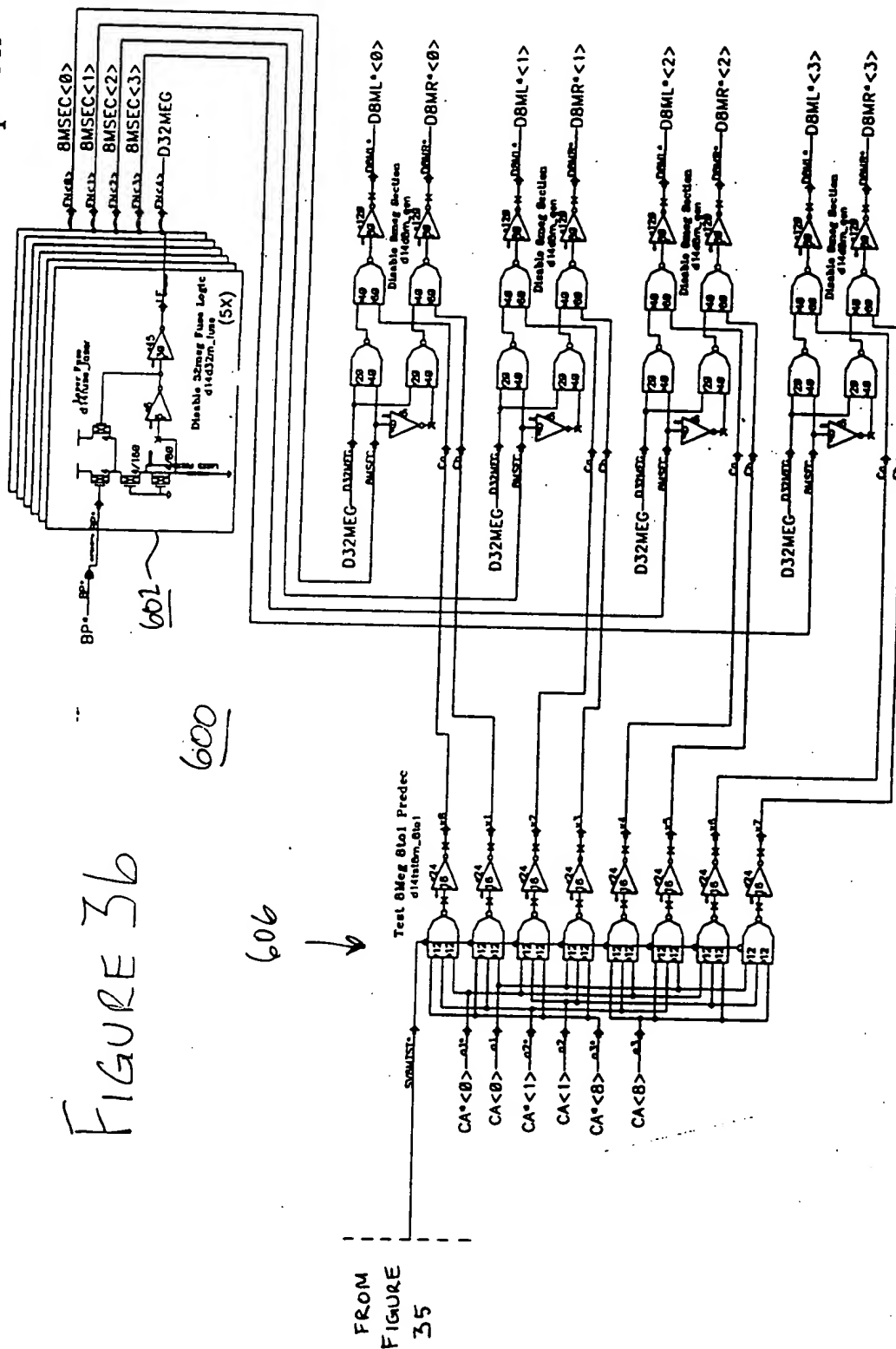
FIGURE 35

604



# Disable 32meg Laser Fuse Option

FIGURE 3b



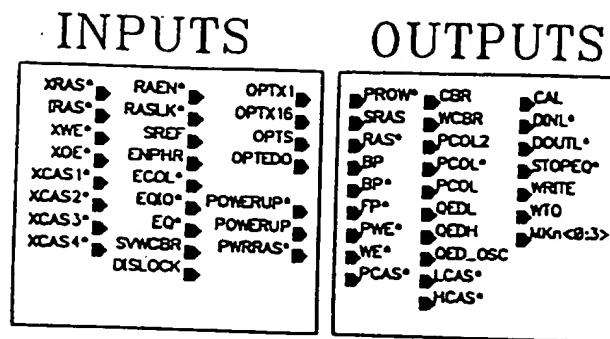


FIGURE 37

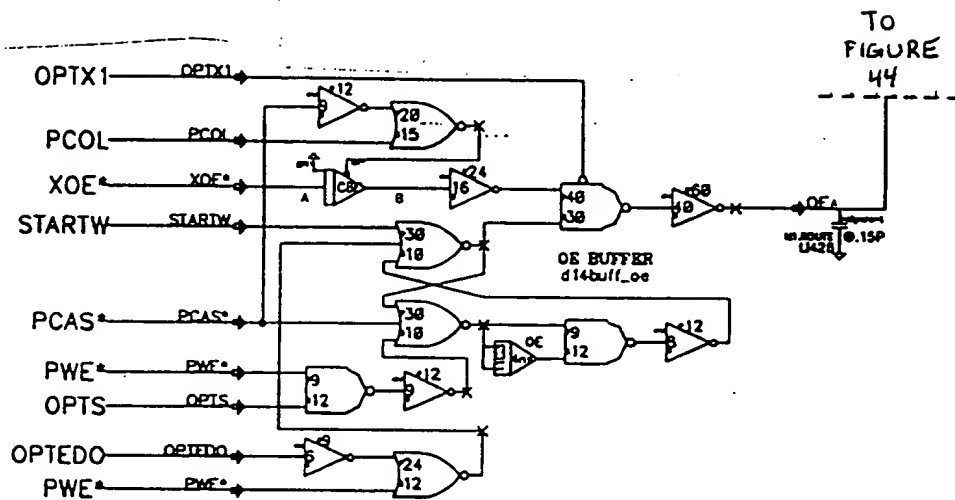


FIGURE 38

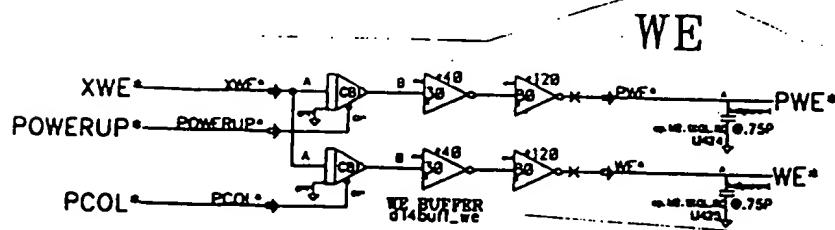


FIGURE 39

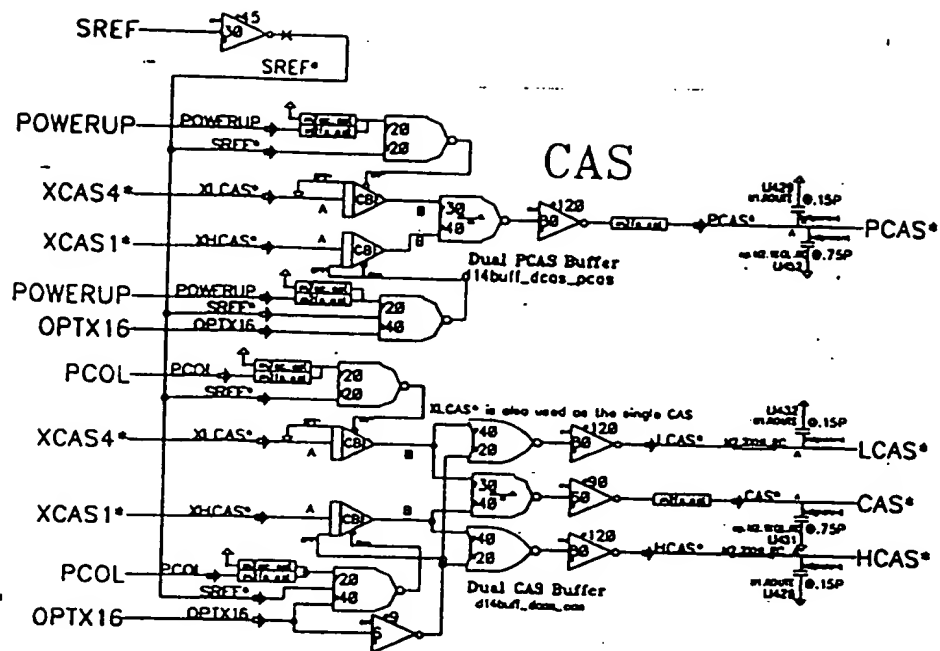


FIGURE 40

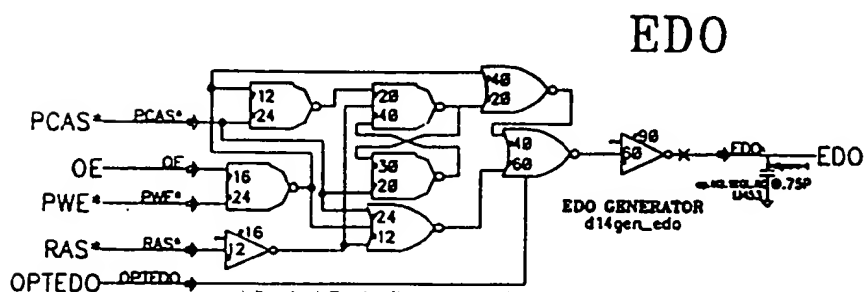


FIGURE 41

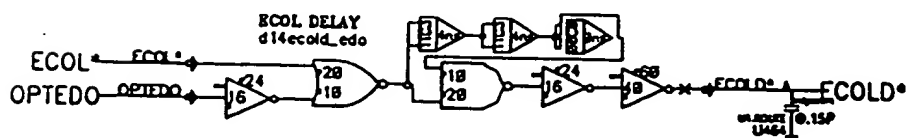


FIGURE 42

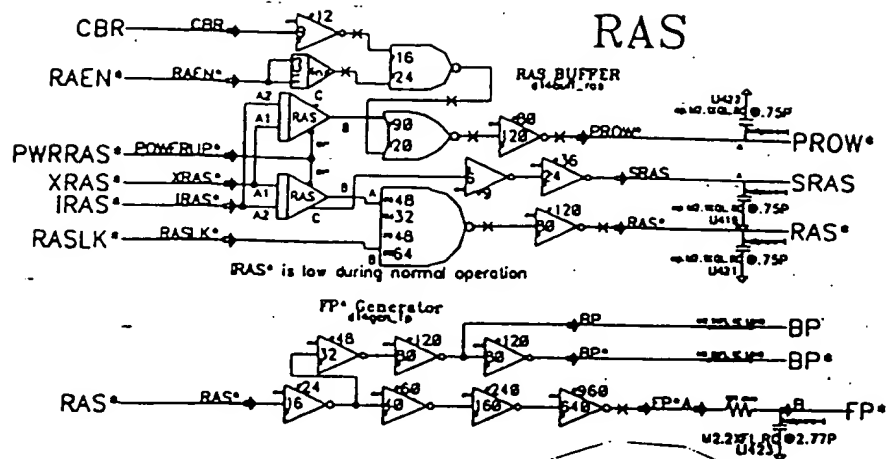


FIGURE 43

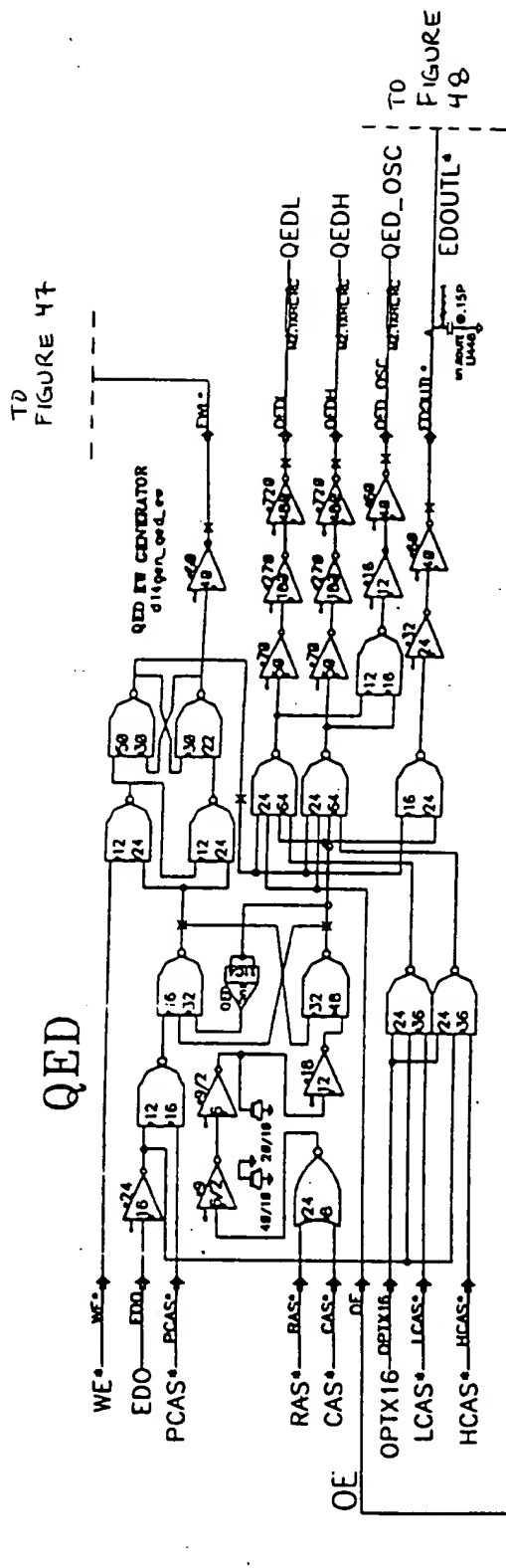


FIGURE 44

FROM  
FIGURE  
38

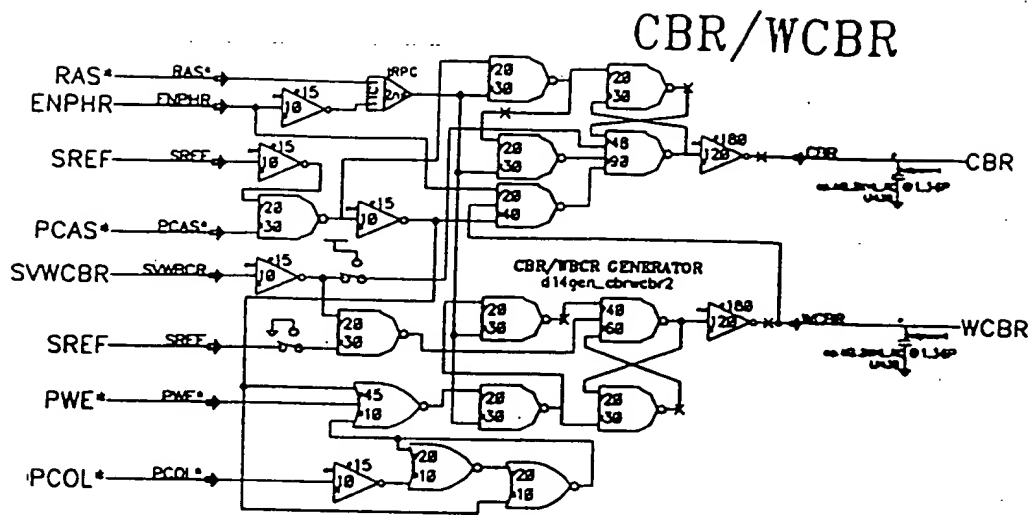


FIGURE 45

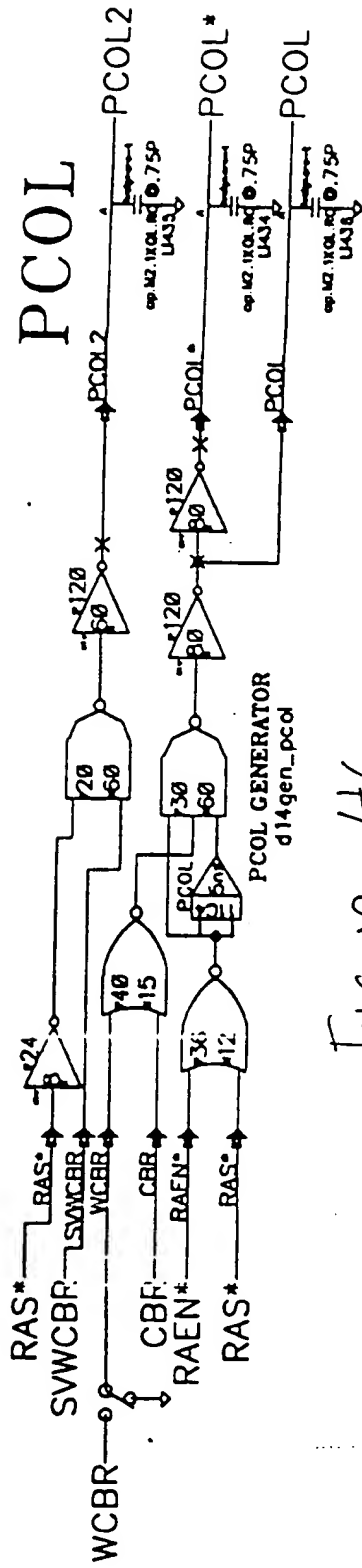


FIGURE 46

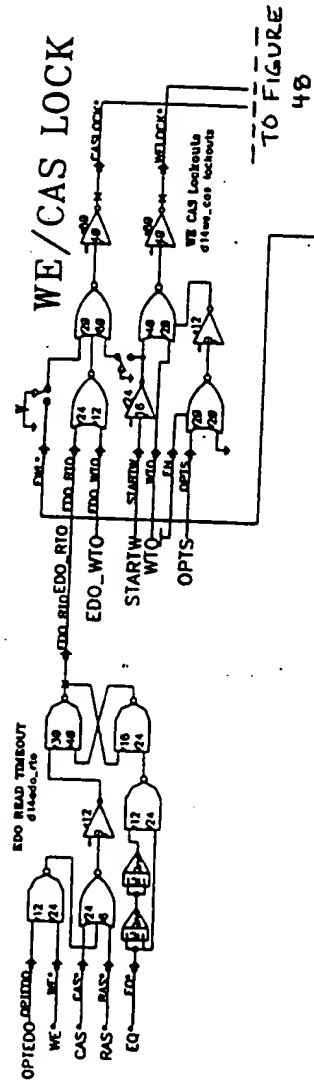


FIGURE 47

FROM  
FIGURE  
47

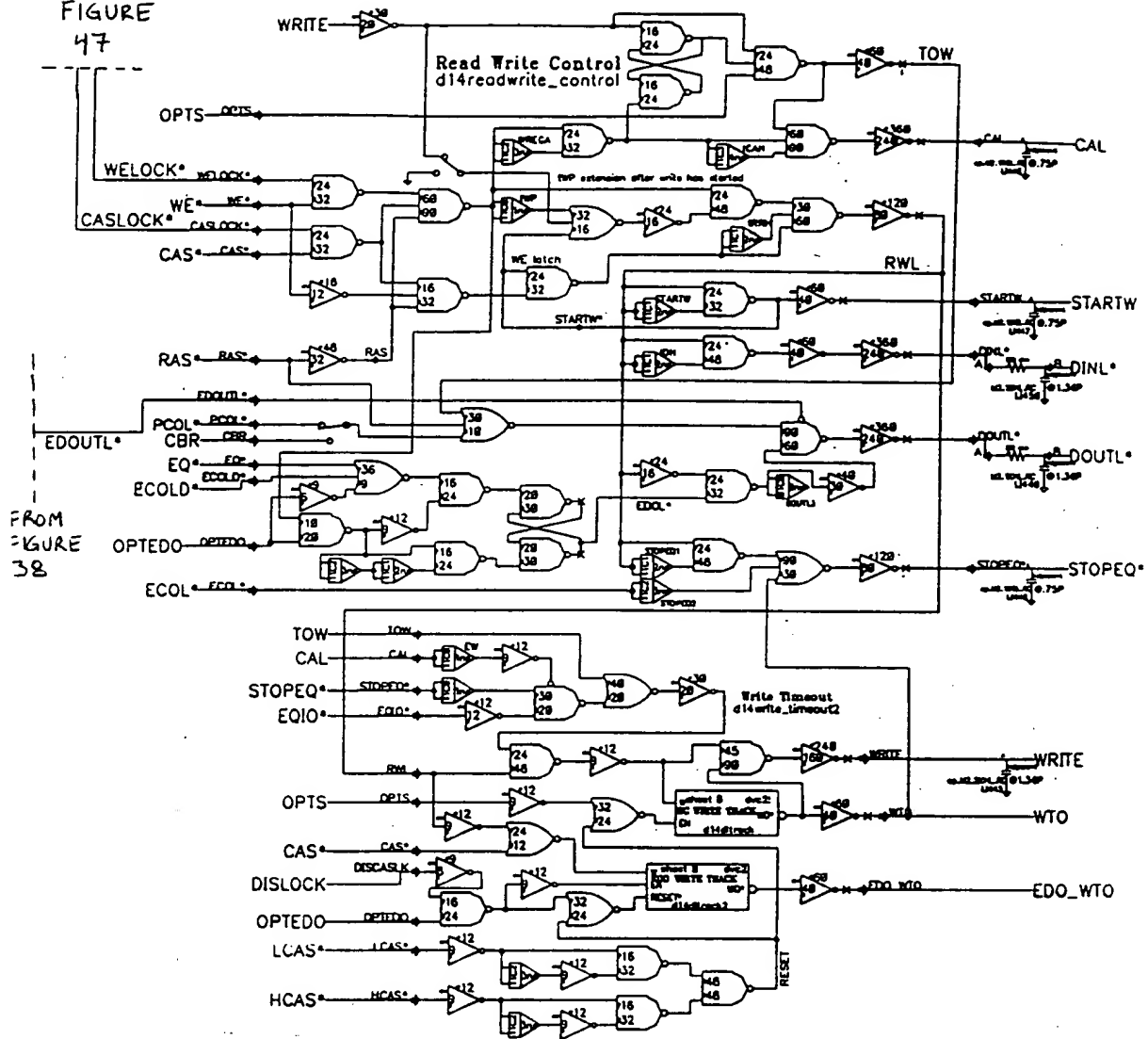


FIGURE 48



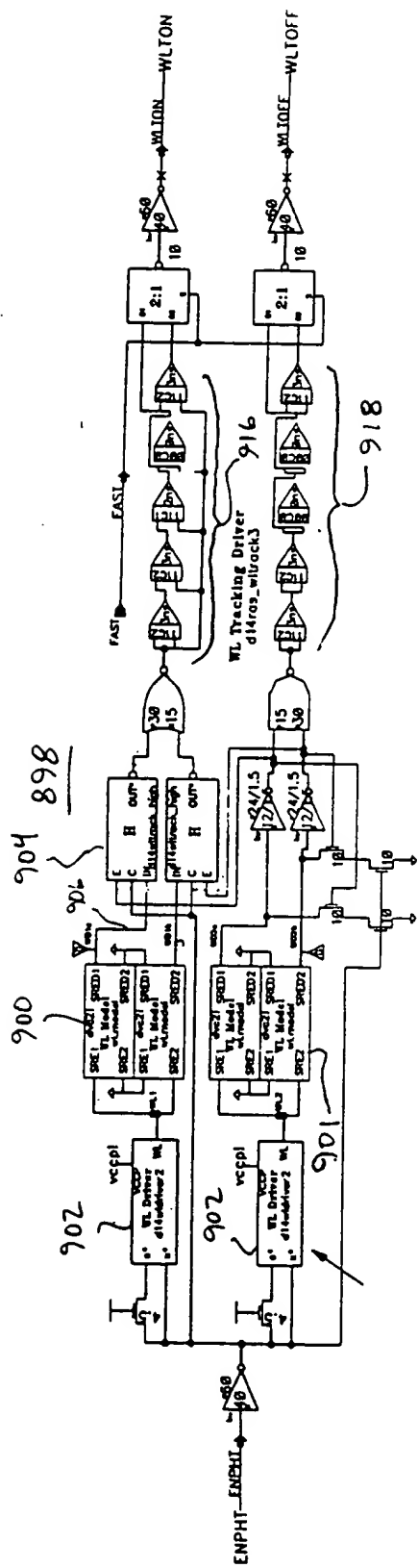


FIGURE 49

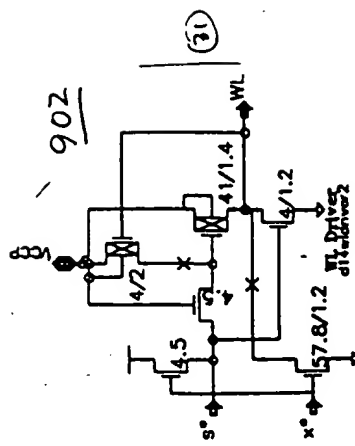


FIGURE 50

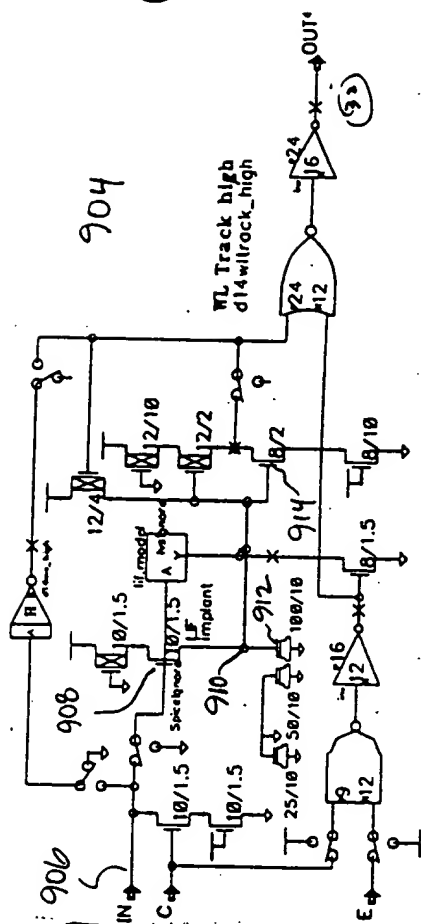
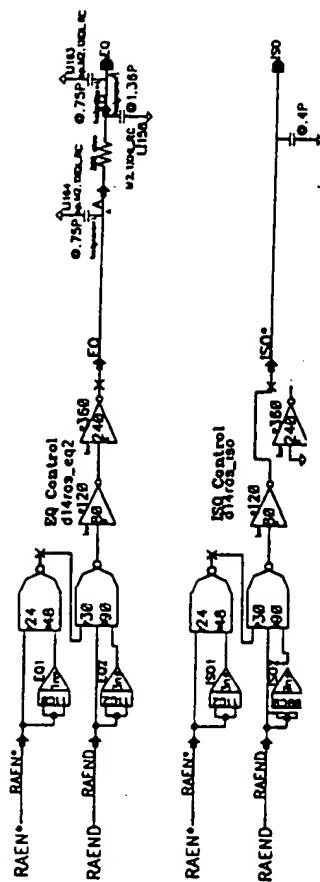
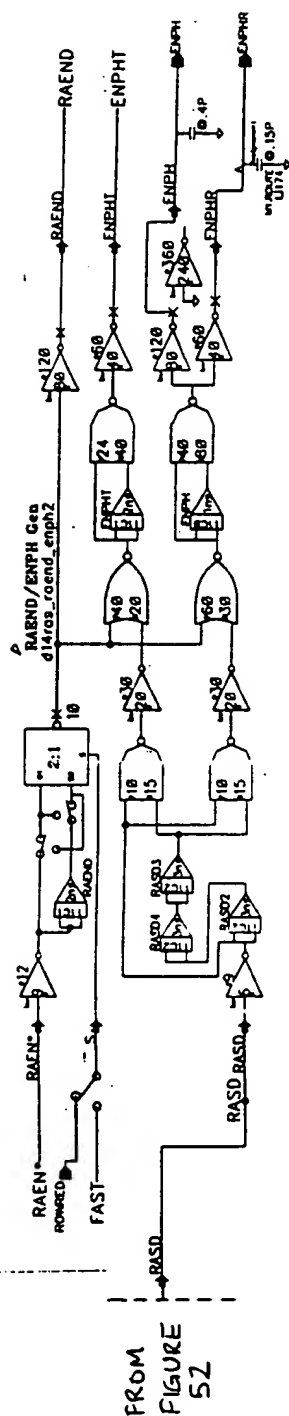


FIGURE 51





920

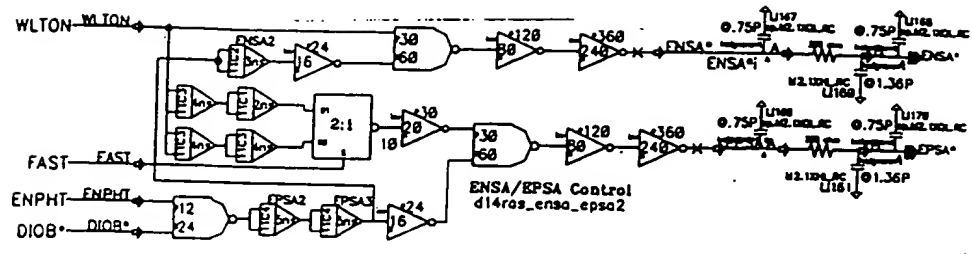


FIGURE 55

## INPUTS

XAS	RAS*
XA7	RAL
XVE*	RAS*
POWERUP*	CBR
CA* <2:7>	WCBR
CA <6>	ENPHR
OPT4KREF	PCAS*
BURNIN	ECBR
032MEG	

## OUTPUTS

DIOB*	MICRON*
SVWCBR	32KTEST
SRTST	64_128X
GNDV8B*	ALLROW
DISV8B*	REDTESTR
TRESET*	REDTESTC
TEST	DISRED*
TX2	DCOMP
SVREF	DISLOCK
SVFID*	4KREF
	AFSTRESS
	DISTOP*
	SREFTST

FIGURE 56

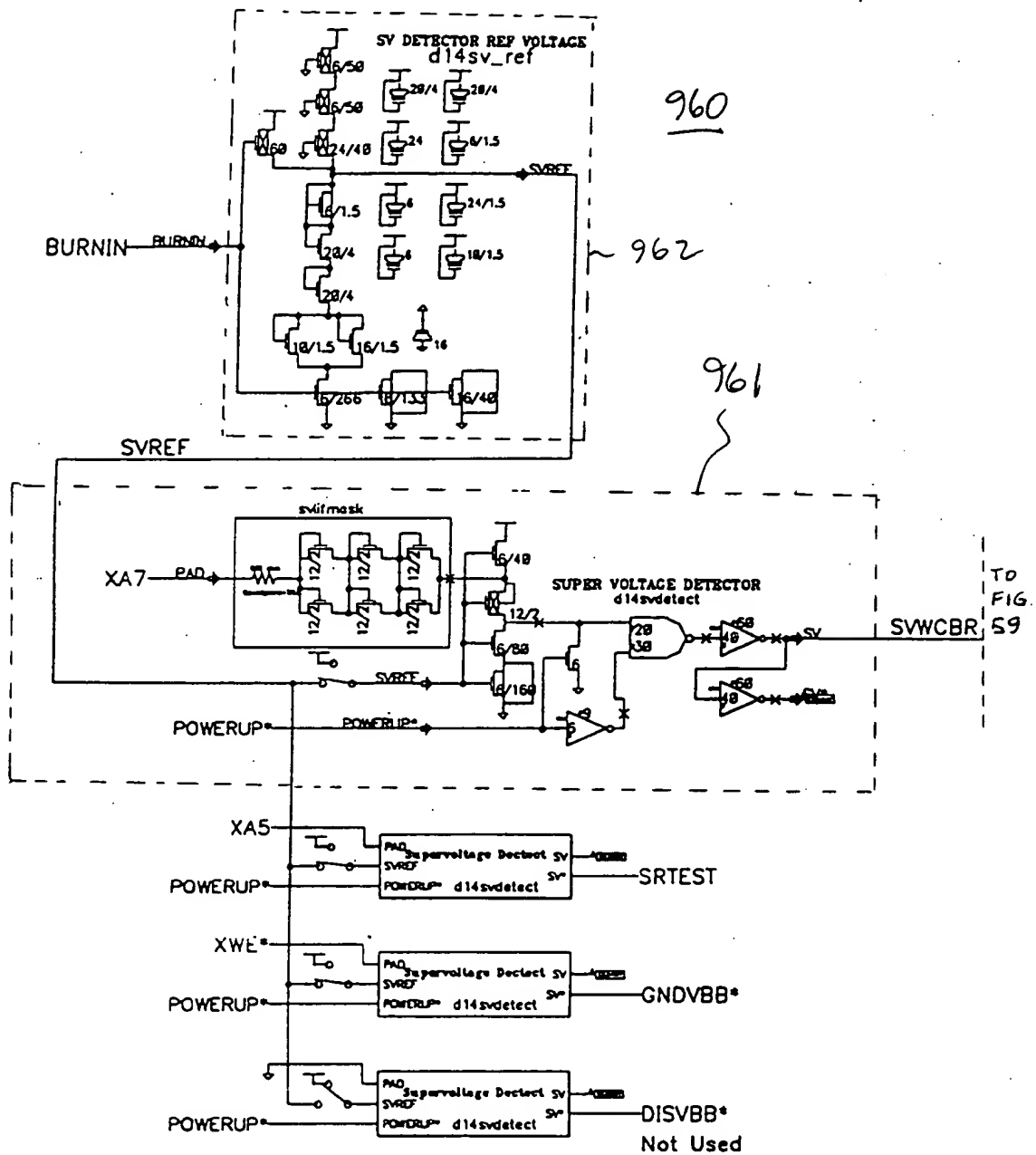


FIGURE 57

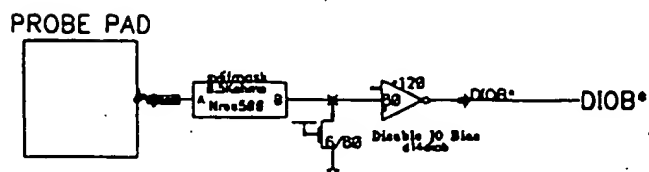


FIGURE 58

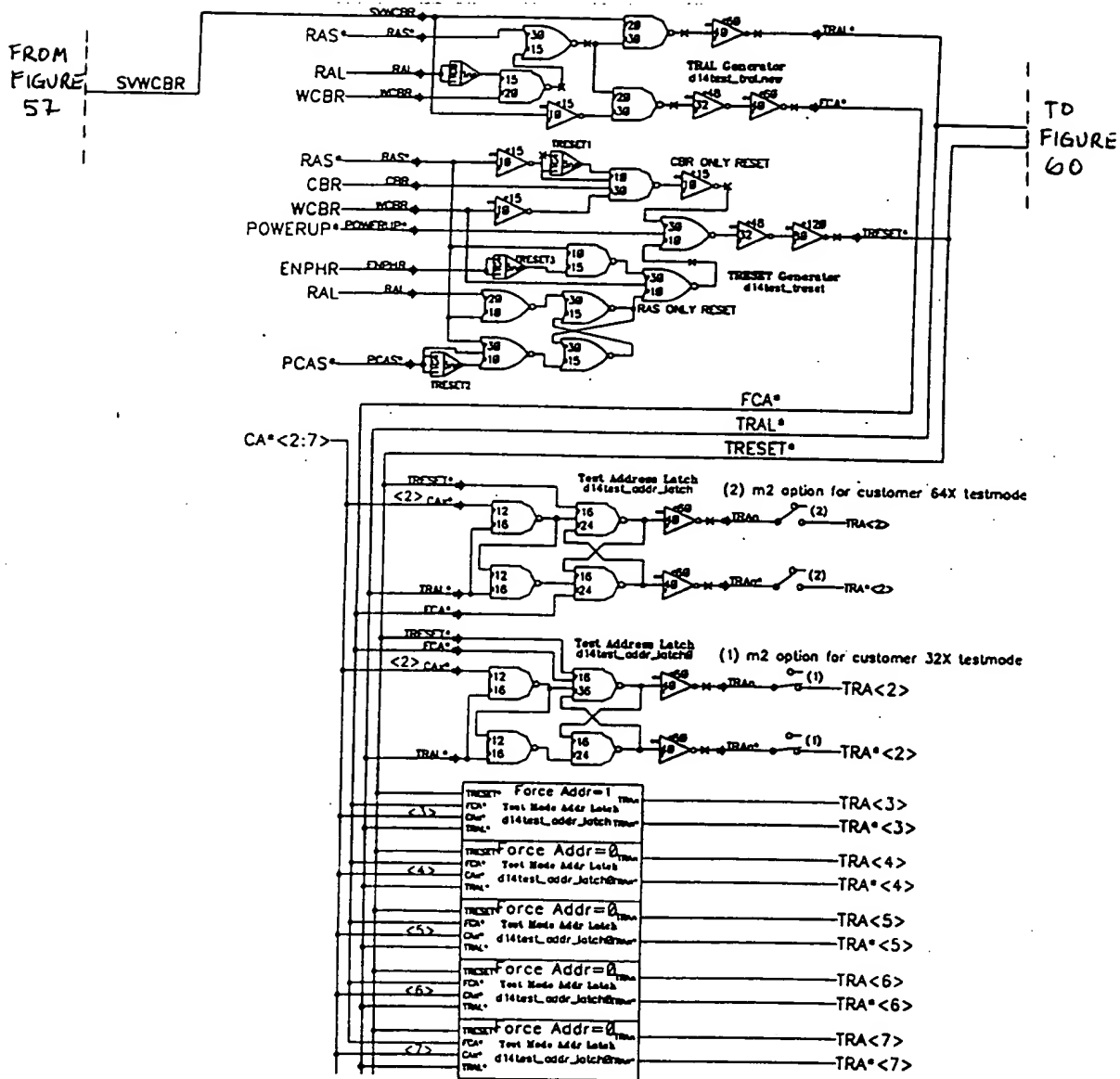


FIGURE 59

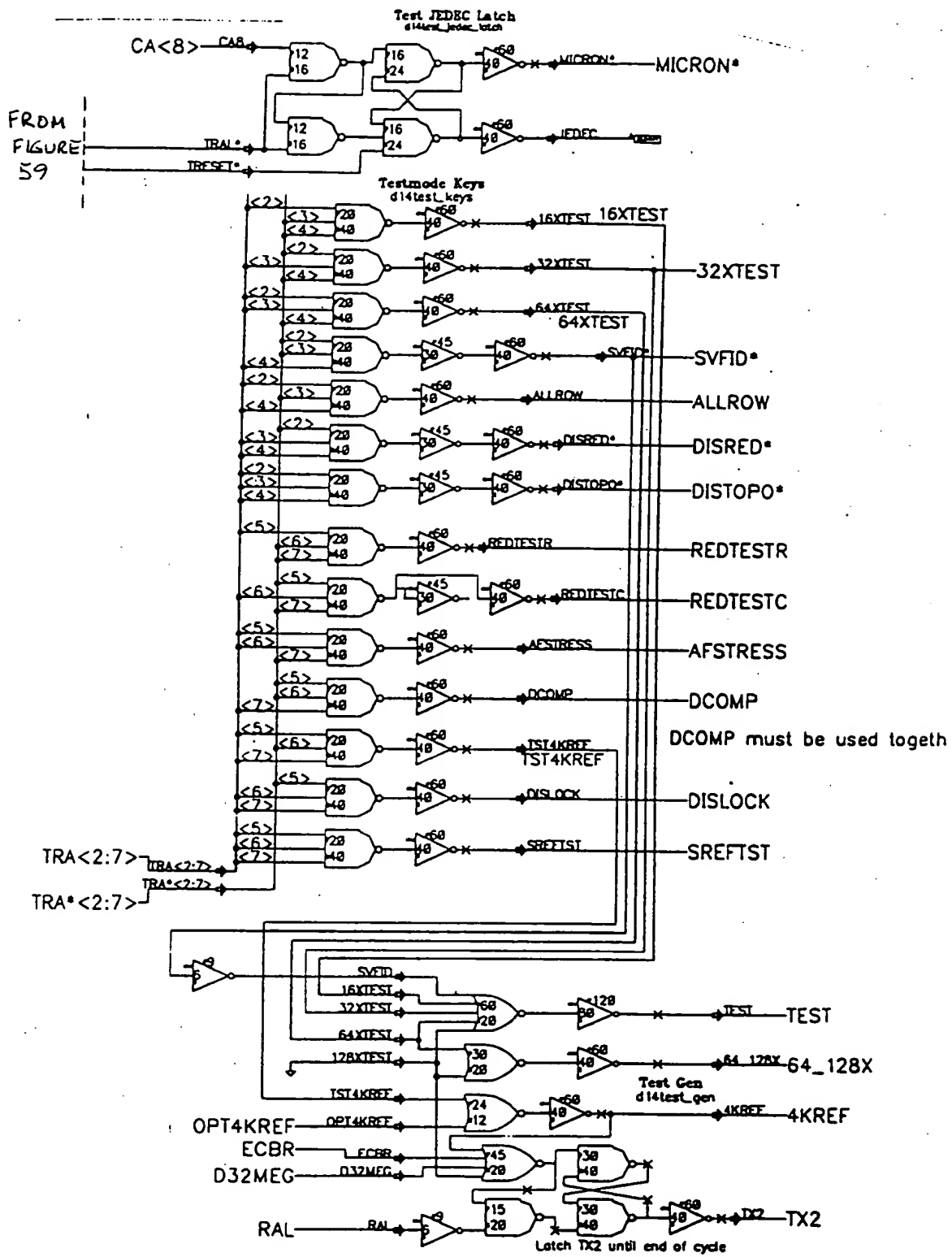


FIGURE 60



### Test Mode Address Keys

A1	A0	A6	A5	A4	A3	A2	TEST MODE
-	-	-	-	0	0	0	no test
-	-	-	-	0	0	1	16X test
-	-	-	-	0	1	0	32X test
-	-	-	-	0	1	1	64X test
-	-	-	-	1	0	0	Fuse I.D.
-	-	-	-	1	0	1	Disable DVC2 w/ all rows high
-	-	-	-	1	1	0	Disable redundant element
-	-	-	-	1	1	1	Disable Data Topo
-	0	0	0	-	-	-	no test
-	0	0	1	-	-	-	Row redundant element pretest
-	0	1	0	-	-	-	Column redundant element pretest
-	0	1	1	-	-	-	Anti-fuse Stress test
-	1	0	0	-	-	-	Test Data compression
-	1	0	1	-	-	-	4K refresh (otherwise 8K ref)
-	1	1	0	-	-	-	Disable RAS/CAS lockout
-	1	1	1	-	-	-	Self-refresh Test
0	-	-	-	-	-	-	JEDEC test mode
1	-	-	-	-	-	-	MICRON test mode

FIGURE 61

### Supervoltage and Backend Programming Inputs

Input Pad	Description of Usage	Page
A0	generates PRGCANR	8
A1	generates PRGCANC	8
A2	generates PRGR	8
A3	generates PRGC	8
A4	supervoltage - Not Used	4a
A5	supervoltage - self refresh test	7
A6	supervoltage - 8Meg ICC test	4b
A7	supervoltage - WCBR	7
A10	anti-fuse programming voltage	8
A11	supervoltage - elect fuse program SVPRG	8
WE	supervoltage - ground VBB	7

FIGURE 62

### JEDEC/MICRON Testmode

READ DATA	OUTPUT	
	JEDEC	MICRON
All 0's	1	0
All 1's	1	1
Different	0	Tristate

FIGURE 63

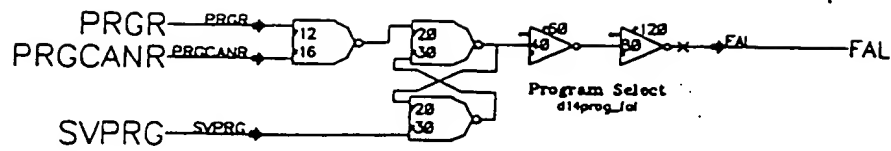


FIGURE 65

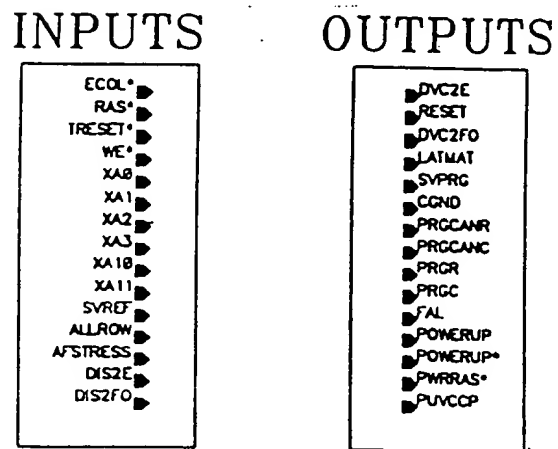


FIGURE 64

# BACKEND REPAIR PROGRAMMING LOGIC

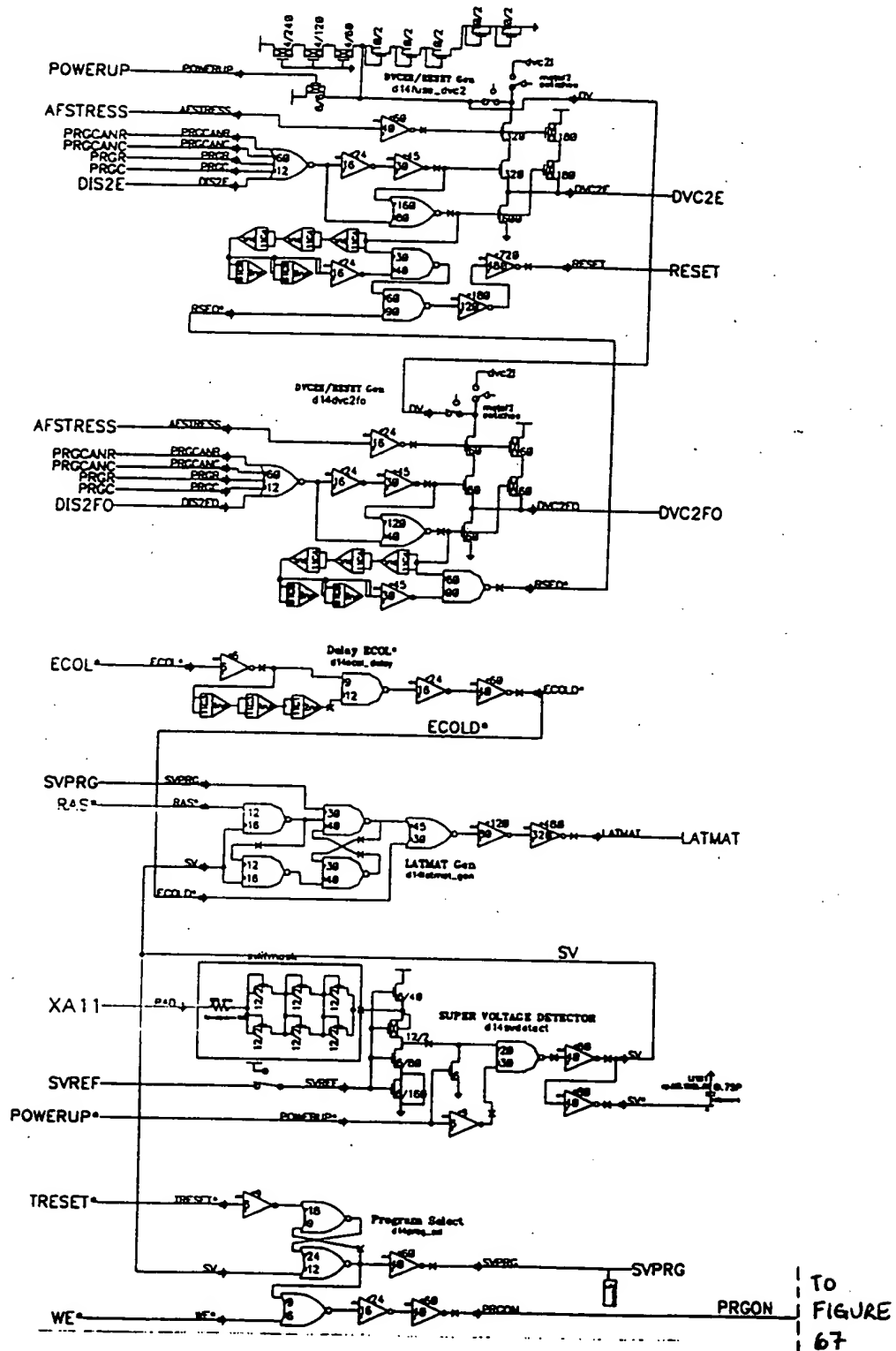


FIGURE 66

SpiceIgnore=TRUE

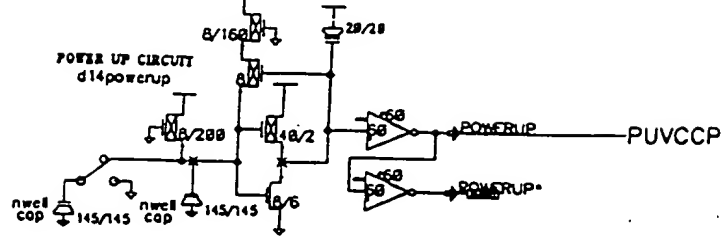


FIGURE 68

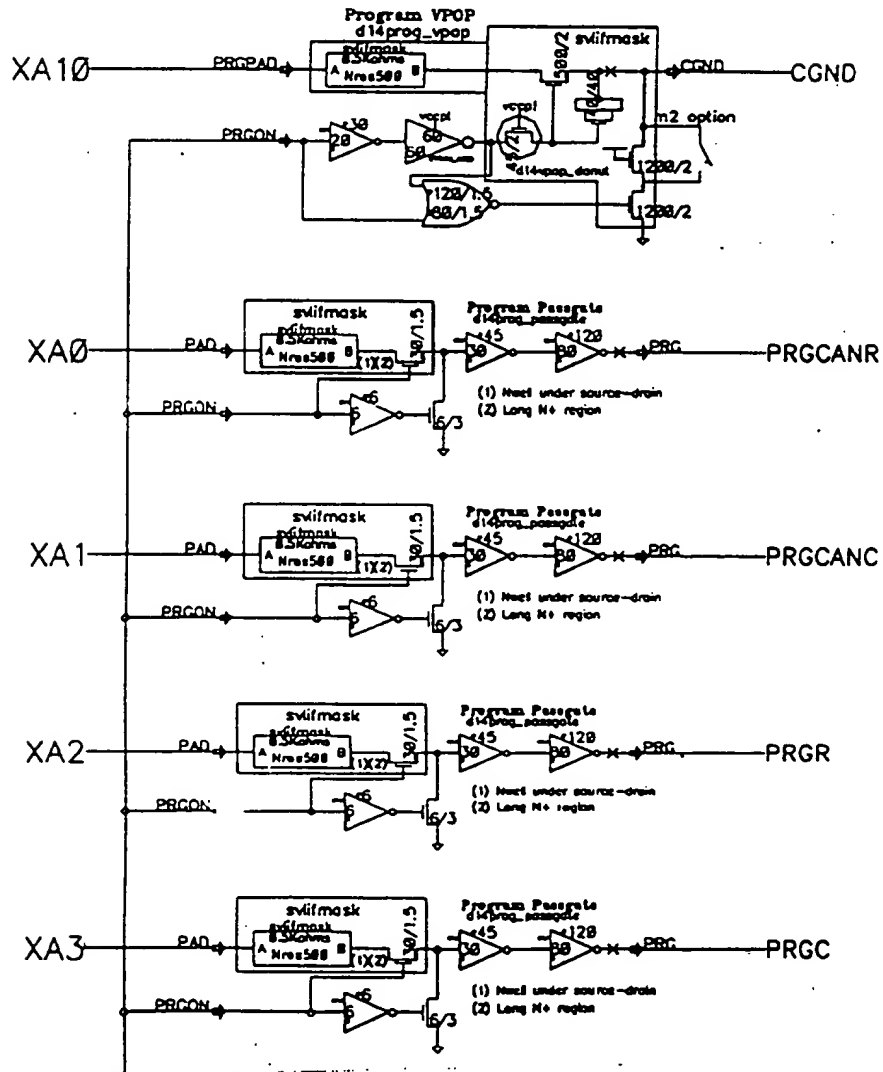


FIGURE 67

## DVC2 Gen

SpiceIgnore=TRUE

Apply Device fixing when LVS'ing

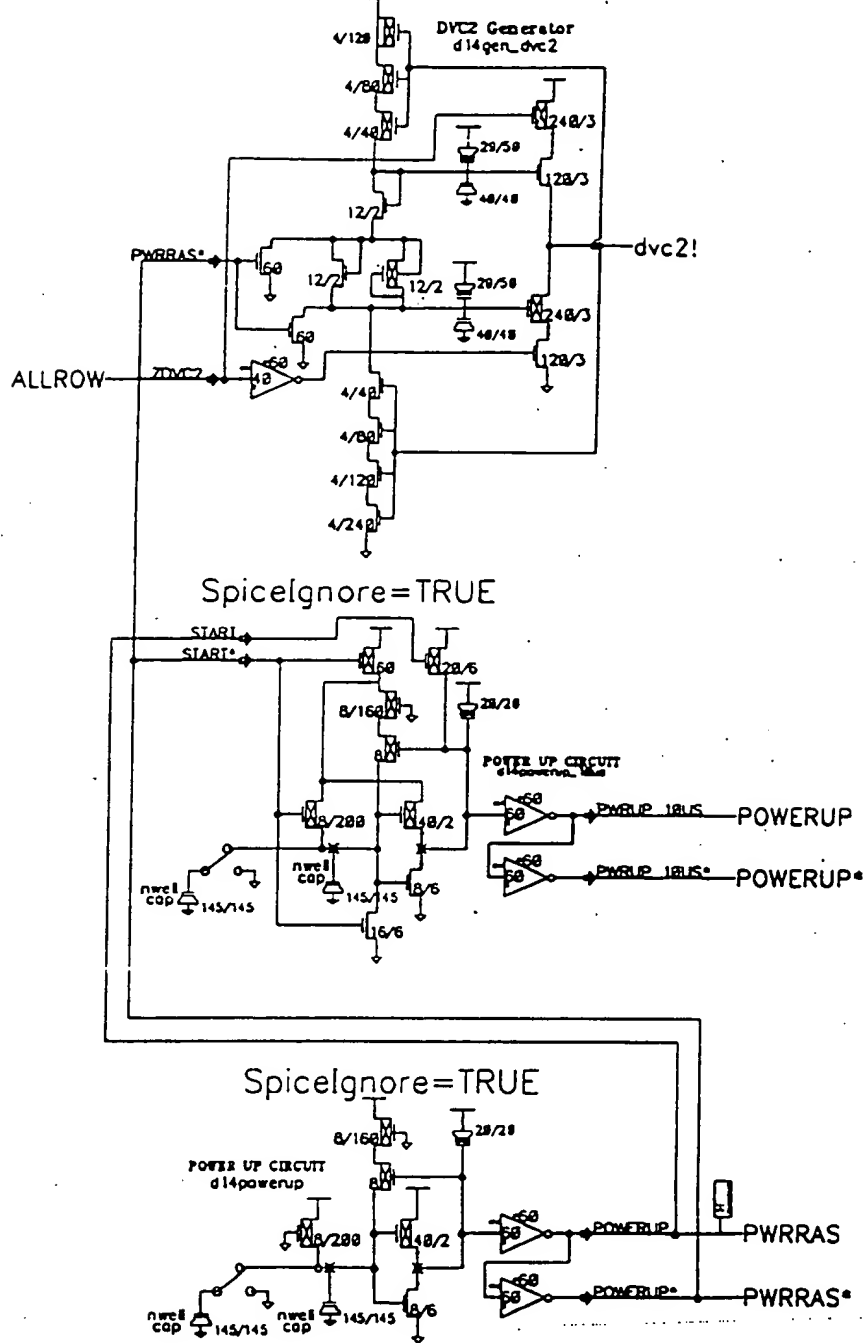


FIGURE 69

# INPUTS      OUTPUTS

RADY*	EVEN
CBR	ODD
RAS*	RA12<0:3>
PROW*	RA34<0:3>
RAL	RA56<0:3>
XA0	RA78<0:3>
XA1	RA910<0:3>
XA2	RA11<0:1>
XA3	RA12<0:1>
XA4	RA<12>
XA5	RA*<12>
XA6	CEVINV
XA7	COOINV
XA8	PRA2*
XA9	PRA3*
XA10	PRA4*
XA11	PRA5*
XA12	PRA6*
TX2	PRA7*
OPT4KREF	EN_OPT
PRGR	RPRE
RAS*	RBPRES
ALLROW	ECBR
ISO	

FIGURE 7D

# CBR COUNTER

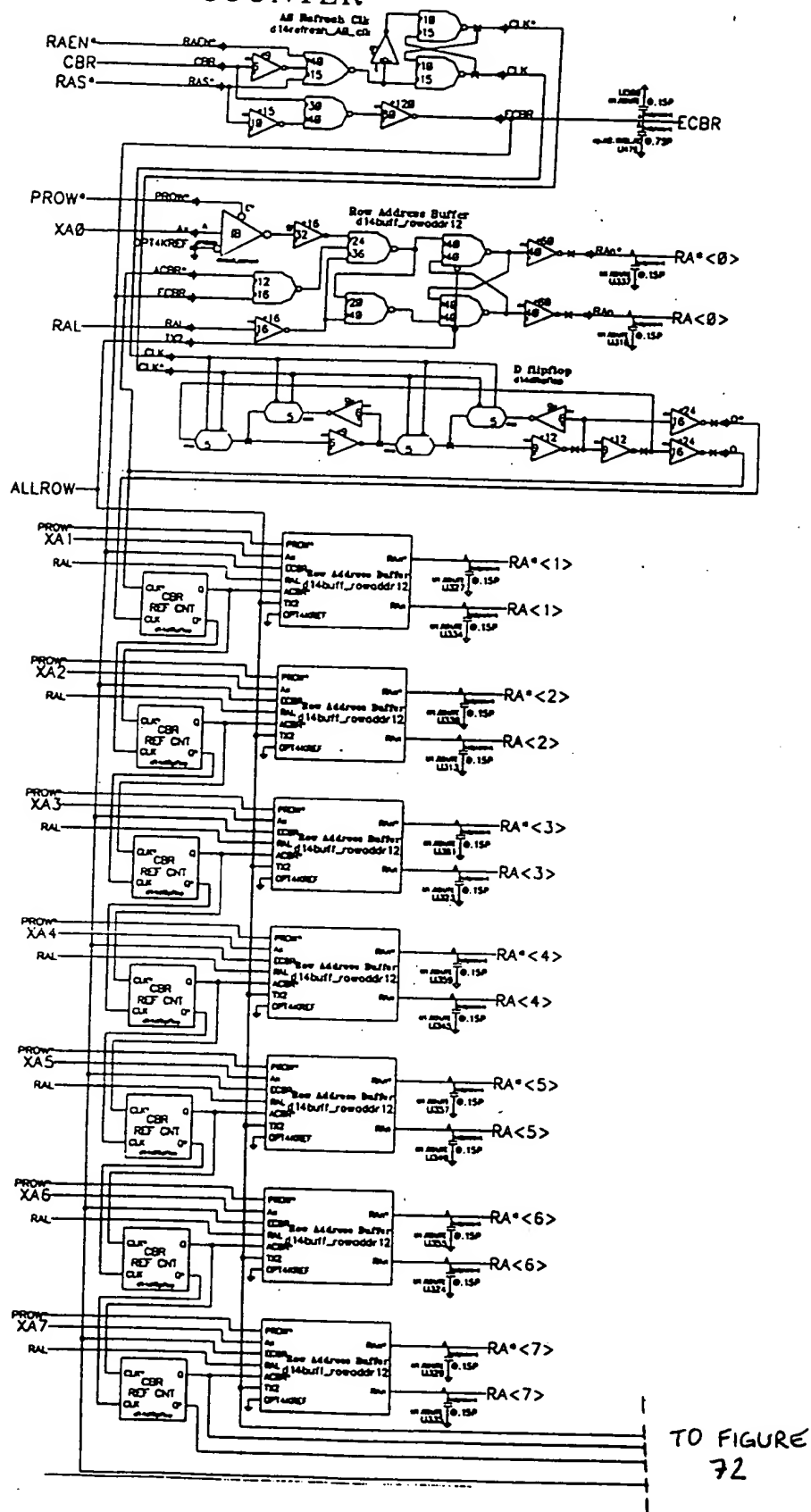


FIGURE 71

# ROW ADDRESS BUFFERS CBR COUNTER

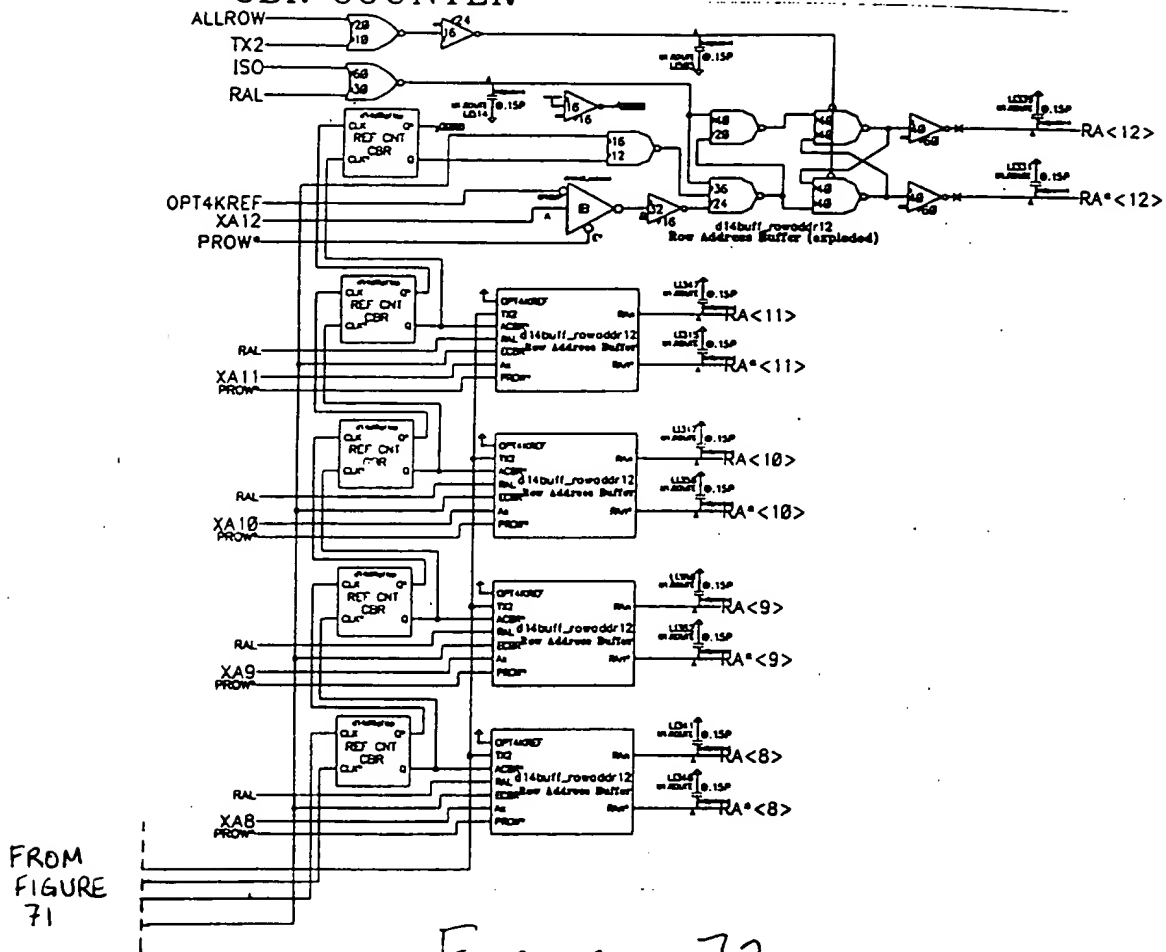
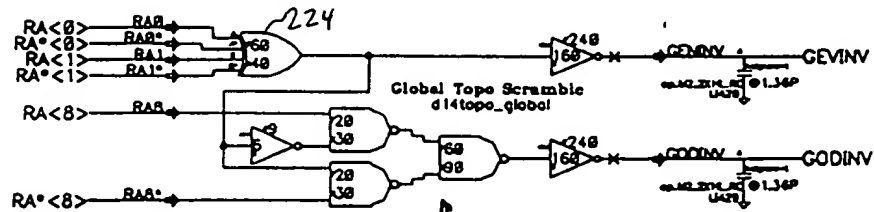


FIGURE 72

22.0  
↓

## GLOBAL TOPO SCRAMBLE



22.6  
FIGURE 73



## FUSE ID ADDRESS

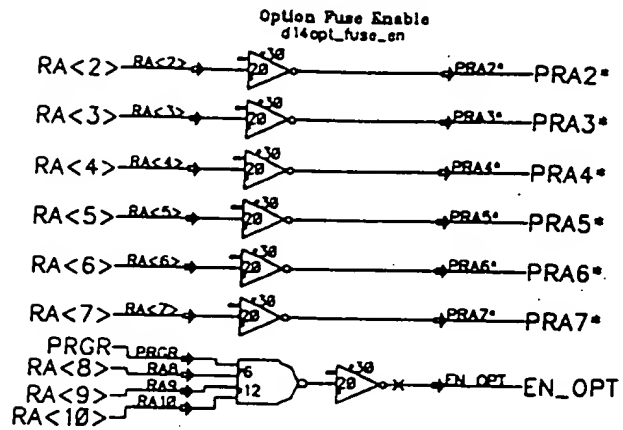


FIGURE 74

## RPRE\*/RBPRES\* GEN

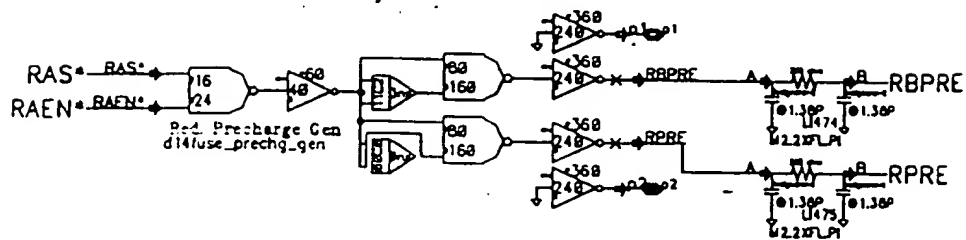
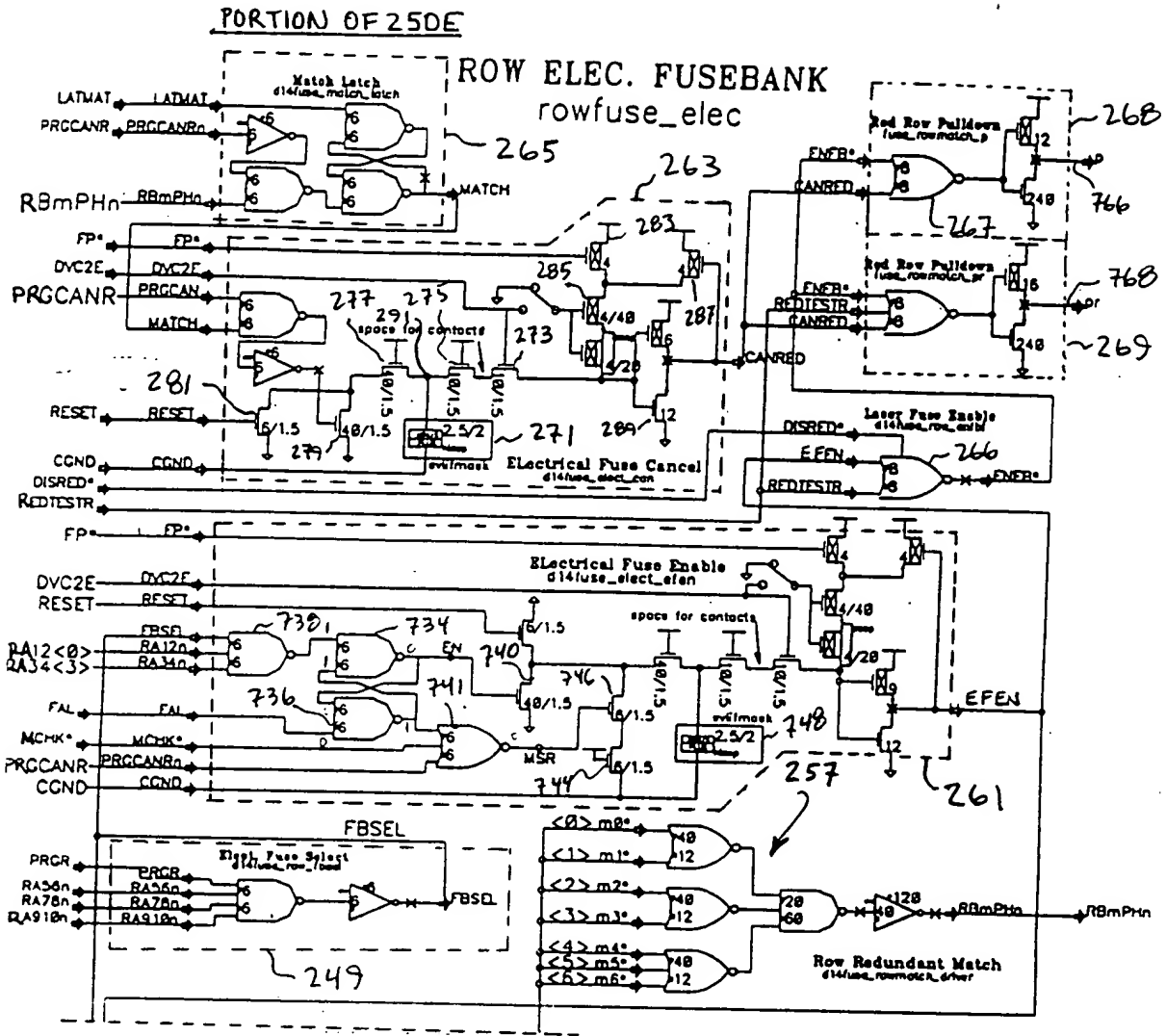


FIGURE 75



TO FIGURE 77

FIGURE 76

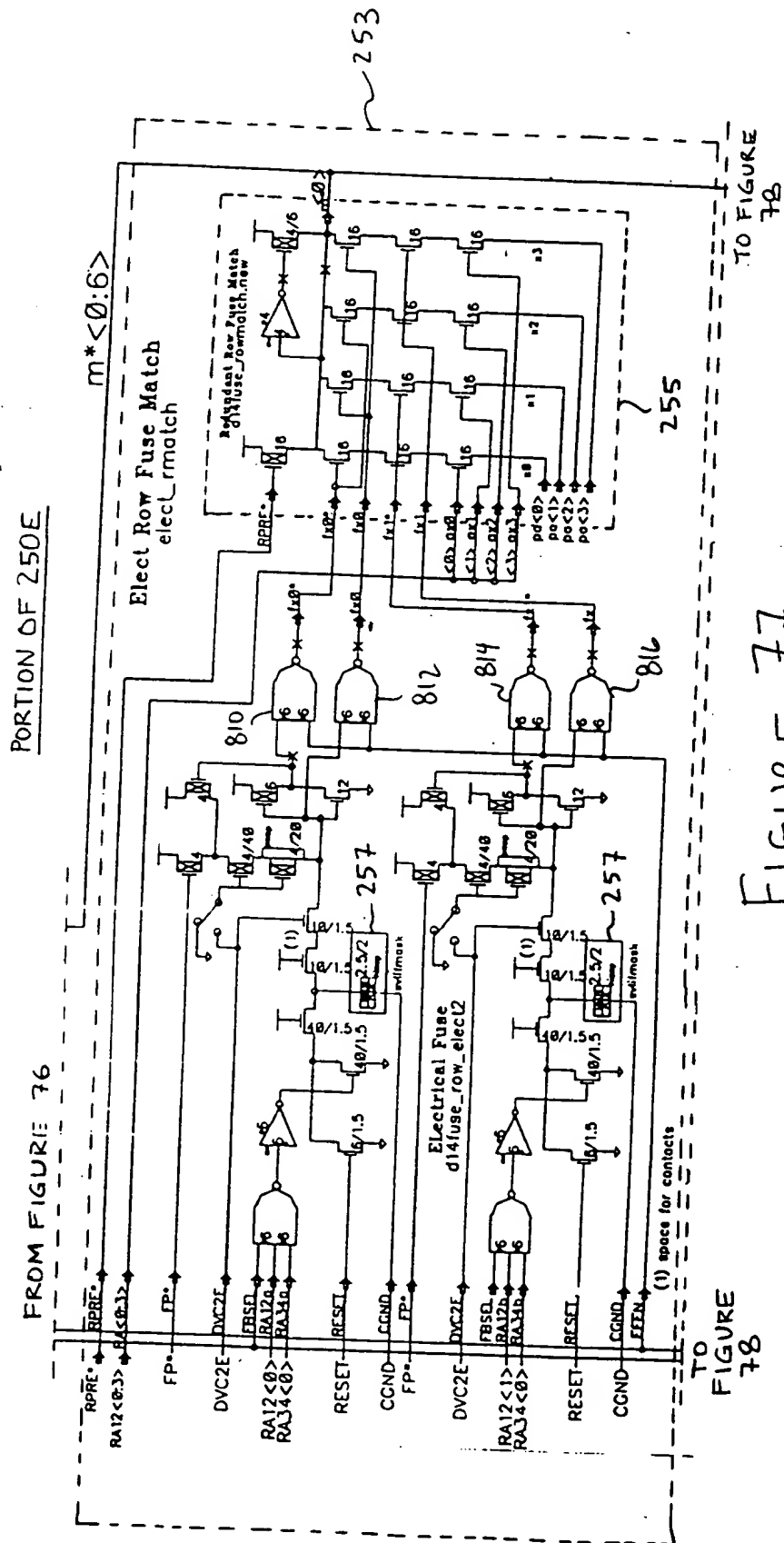


FIGURE 77



FROM  
FIGURE  
77

FROM  
FIGURE  
77

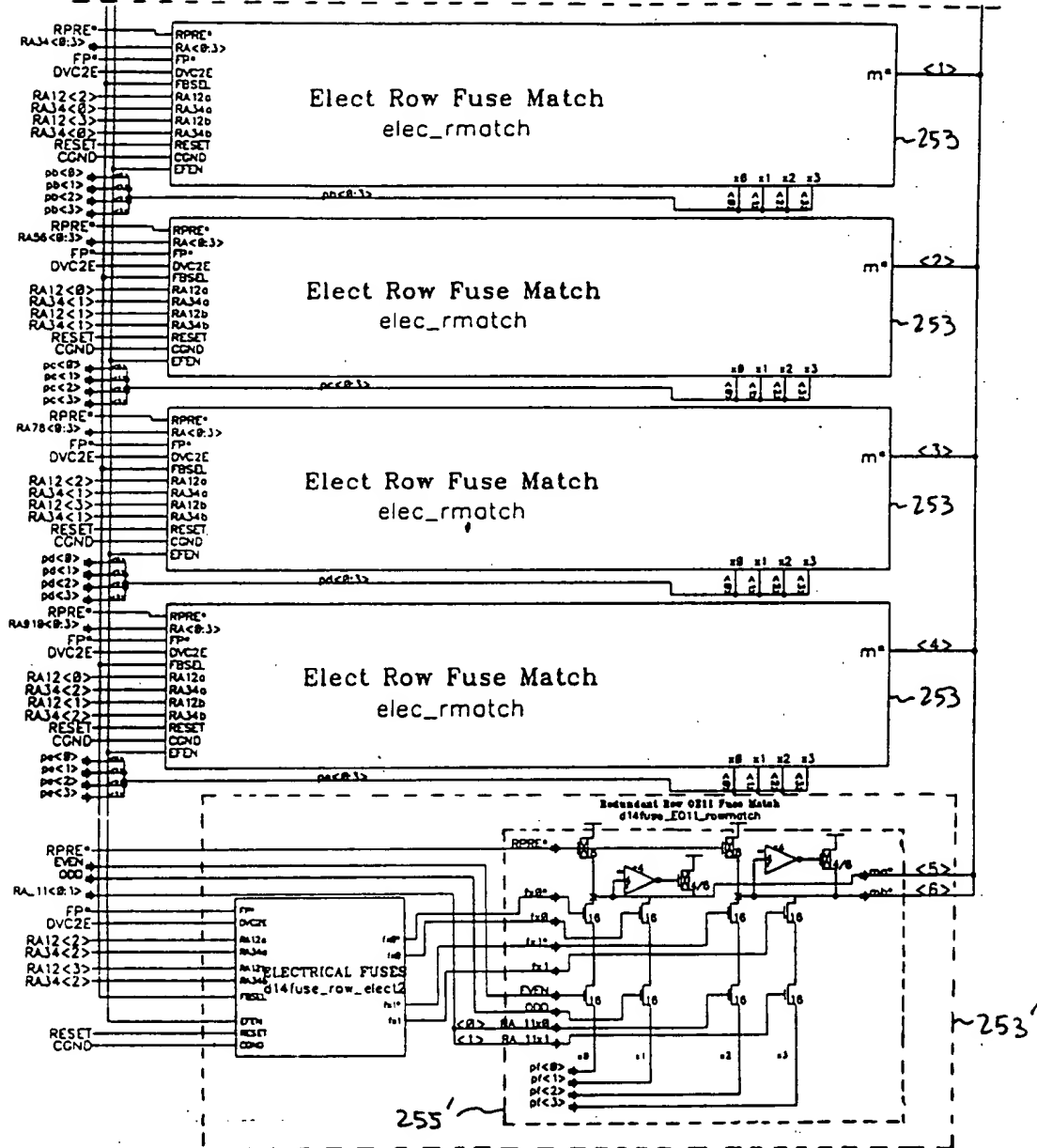


FIGURE 70

## INPUTS

FP*	RPRE*_L
DVC2E	RPRE*_R
RESET	RA12<0:3>
CGND	RA34<0:3>
REDTESTR	RA56<0:3>
DISRED*	RA78<0:3>
PRGCANRT	RA910<0:3>
PRGCANRB	RA_11<0:1>
PRGR	EVEN
LATMAT	ODD
FAL	RA910n

## OUTPUTS

RB0PH_B<0:3>	RB0PH_T<0:3>
RB1PH_B<0:3>	RB1PH_T<0:3>
RB2PH_B<0:3>	RB2PH_T<0:3>
RB3PH_B<0:3>	RB3PH_T<0:3>
RB4PH_B<0:3>	RB4PH_T<0:3>
RB5PH_B<0:3>	RB5PH_T<0:3>
RB6PH_B<0:3>	RB6PH_T<0:3>
RB7PH_B<0:3>	RB7PH_T<0:3>
RAB78_L<0:3>	RAB78_R<0:3>
RAB910_L<0:3>	RAB910_R<0:3>
RAB_11_L<0:1>	RAB_11_R<0:1>

FIGURE 80

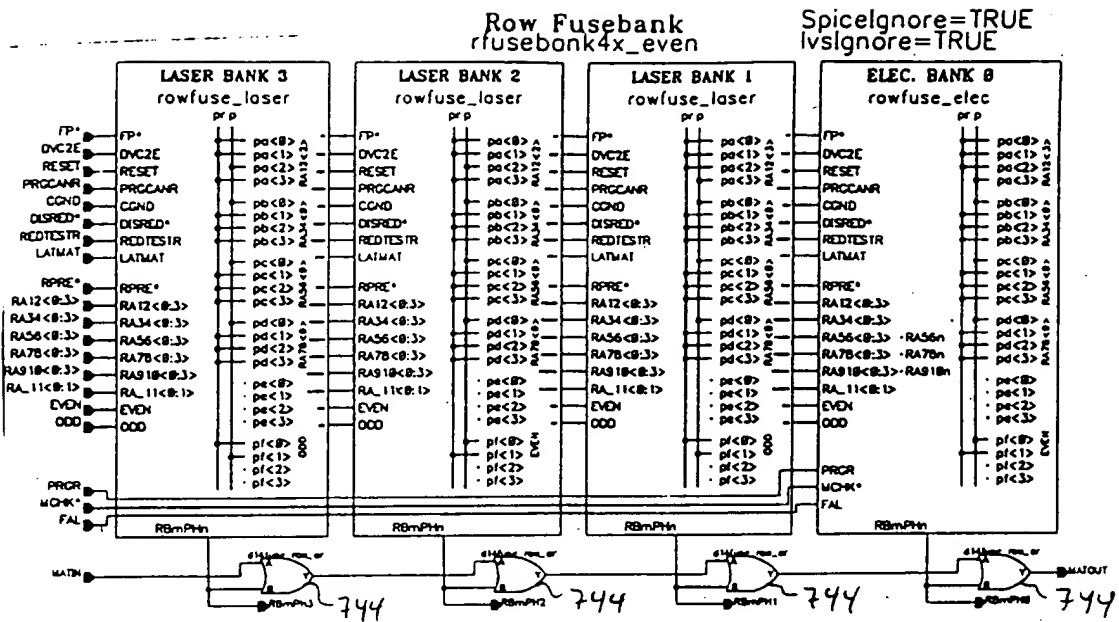


FIGURE 81

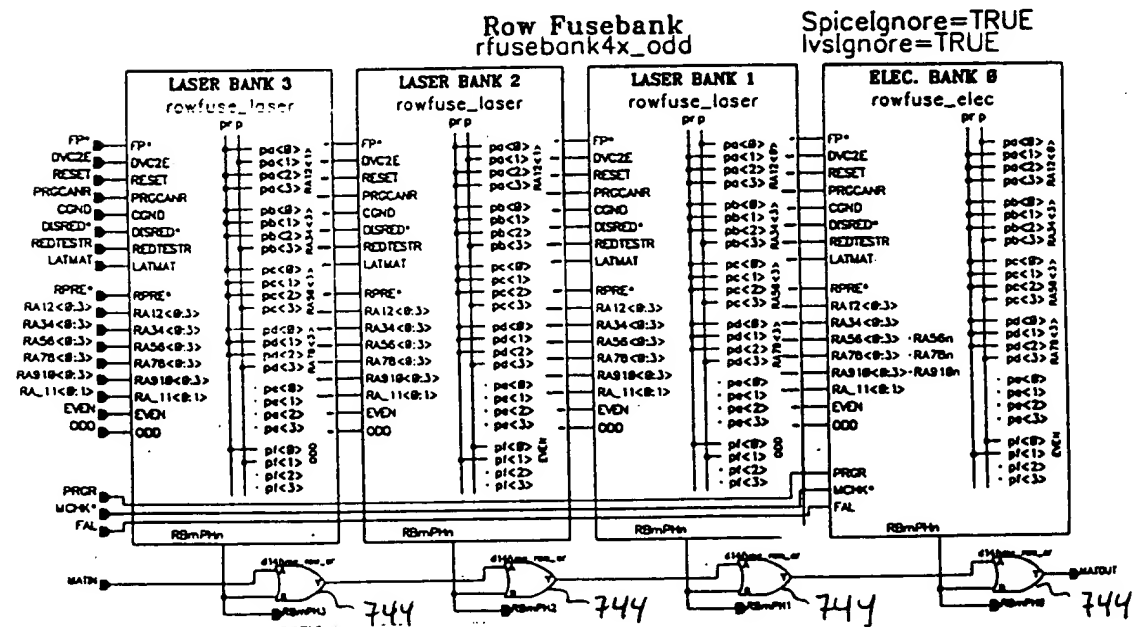


FIGURE 82

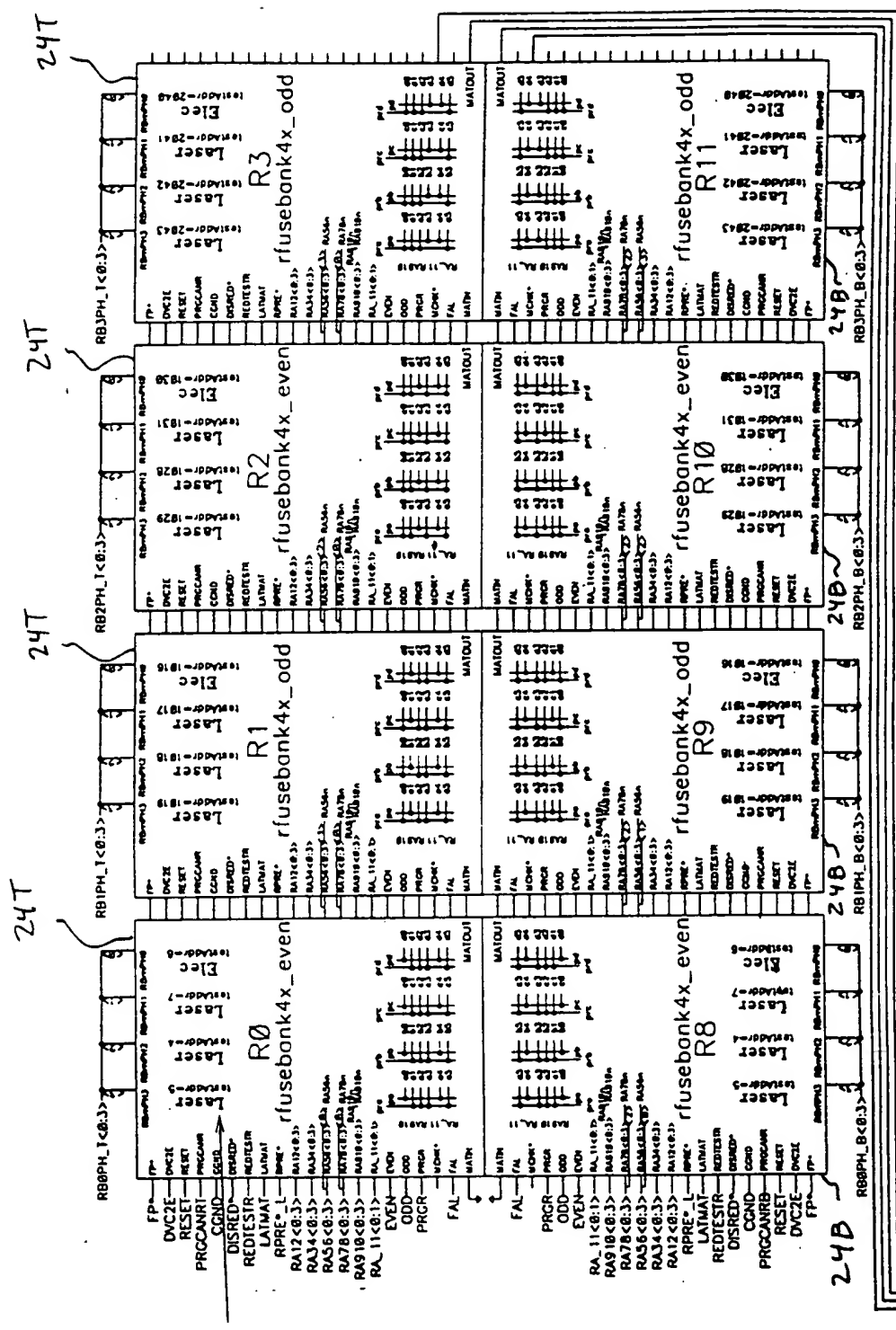


FIGURE 83

TO  
FIGURE  
84



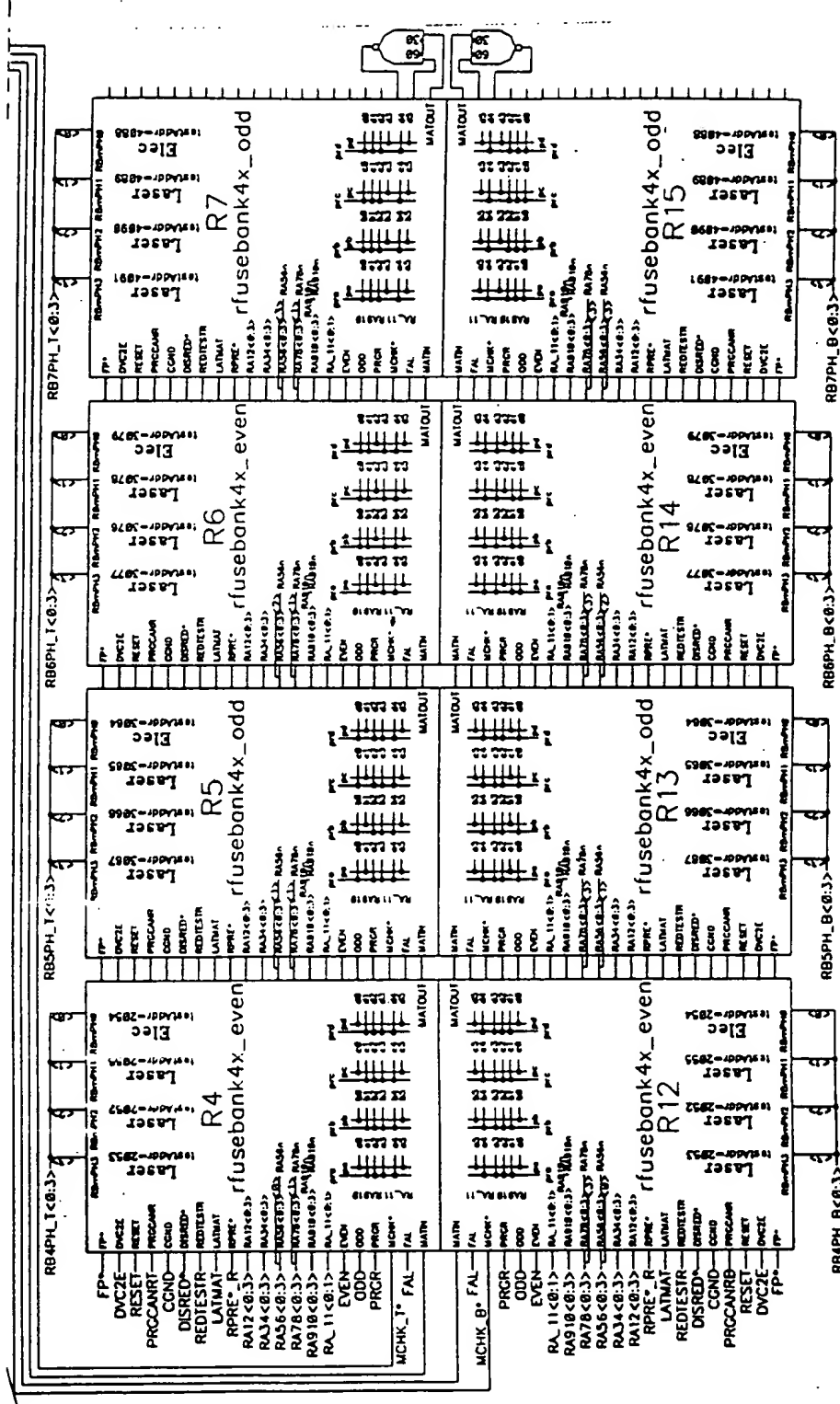


FIGURE 84

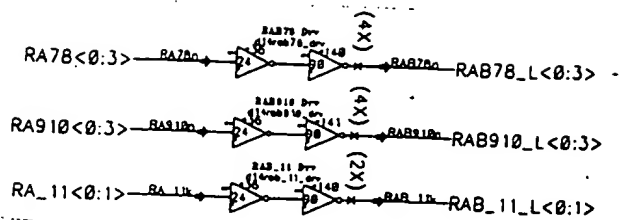


FIGURE 85

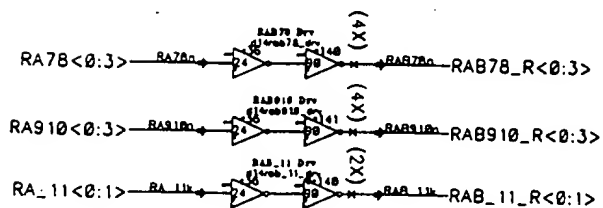


FIGURE 86

## INPUTS

XA0	PCOL*	STOPE0*
XA1	PCOL	DIOB*
XA2	PCOL2	COLRED
XA3	RAL	
XA4	CAL	OPTX4
XA5	TEST	OPTX8
XA6	SVPRG	OPTX16
XA7	32XTEST	OPTX8X16
XA8	64_128X	4KREF
XA9	ECOL*	OPTED0
XA10	RA<12>	D32MEG
XA11	RA* <12>	SVBMTST
XA12	ISO	ENPH

## OUTPUTS

CA<0:8>
CA* <0:8>
CA910<0:3>
SELBM<0:1>
PRG910<0:3>
EQIO*
EQSA*
EO*
CA9k
CA9k*
JSO* <0:1>
ENPH* <0:1>

FIGURE 87

# COLUMN ADDRESS BUFFERS/ATD

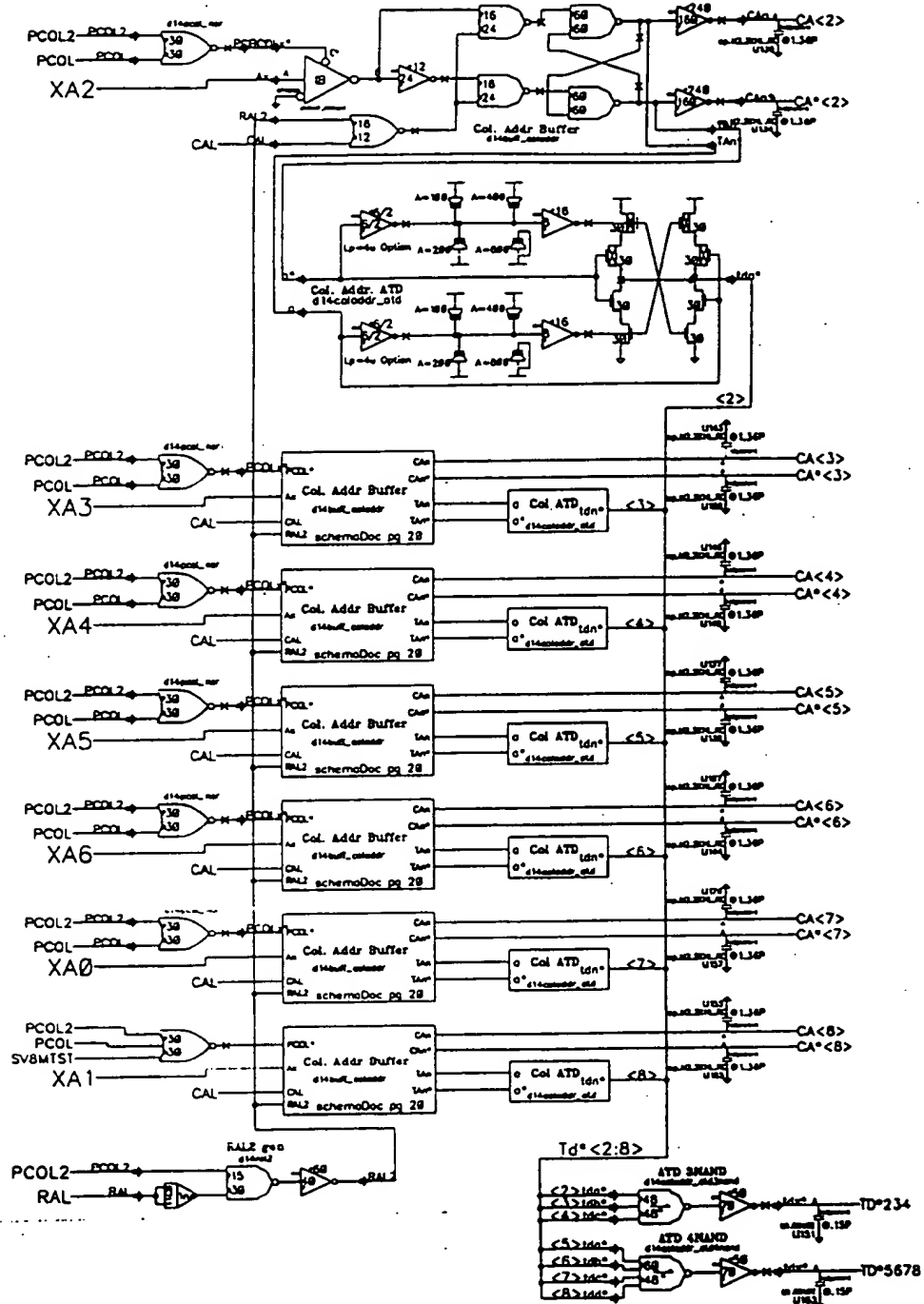


FIGURE 89



CONFIG	ROW ADDRESS	COLUMN ADDRESS
	8K ref	4K ref
4MX16	A0 - A12	A0 - A8
8MX8	A0 - A12	A0 - A9
16MX4	A0 - A12	A0 - A10
64MX1	A0 - A12	A0 - A11
	A0 - A12	A0 - A12

Test Mode Address Compression (ref to X1)	-
16X	A12, A11, A10, A9
32X	A12, A11, A10, A9, A8
64X	A12, A11, A10, A9, A8, A7
128X	A12, A11, A10, A9, A8, A7, RA12

The following column addresses are ignored

FIGURE 88

## 4KREF IGNORE

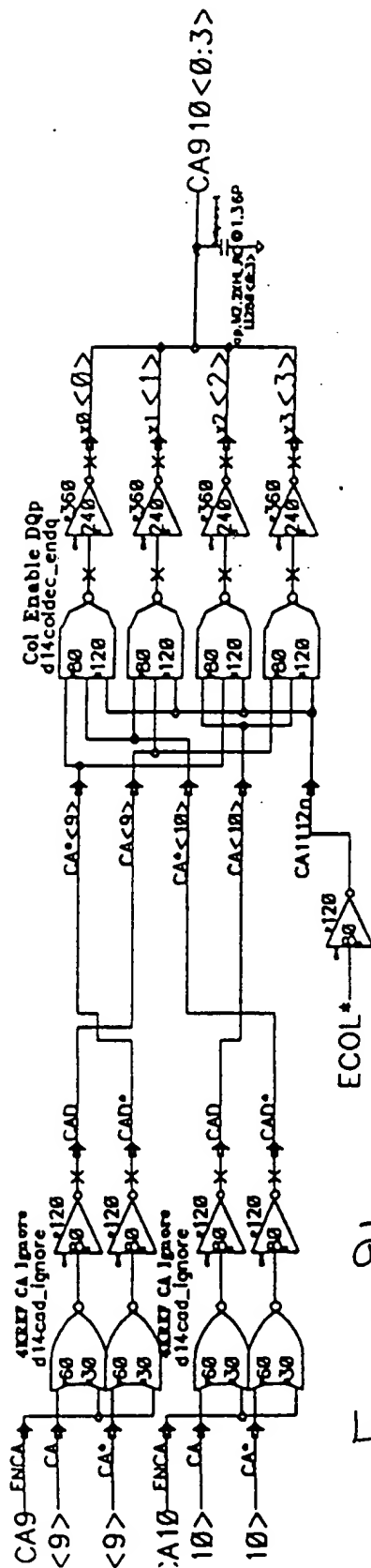


FIGURE 91

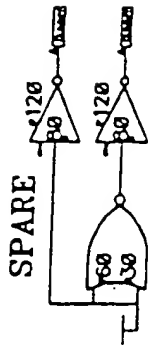


FIGURE 92

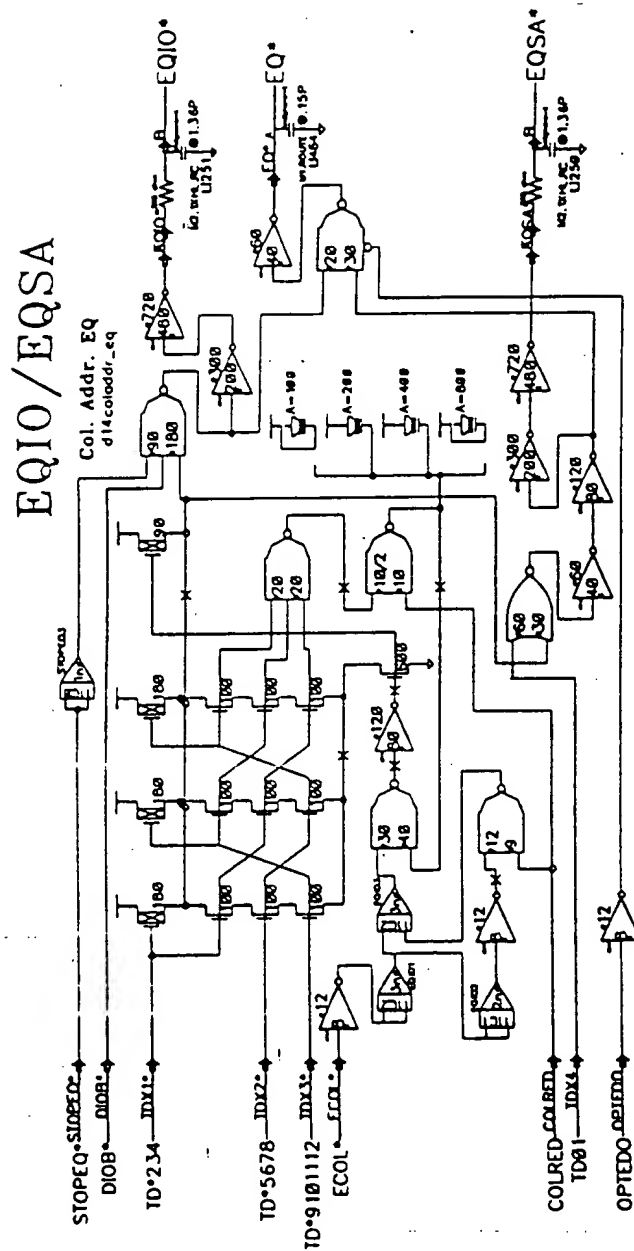


FIGURE 93





FOR BACKEND PROG. ONLY

PRG910 Predec  
d14prdec\_CA910

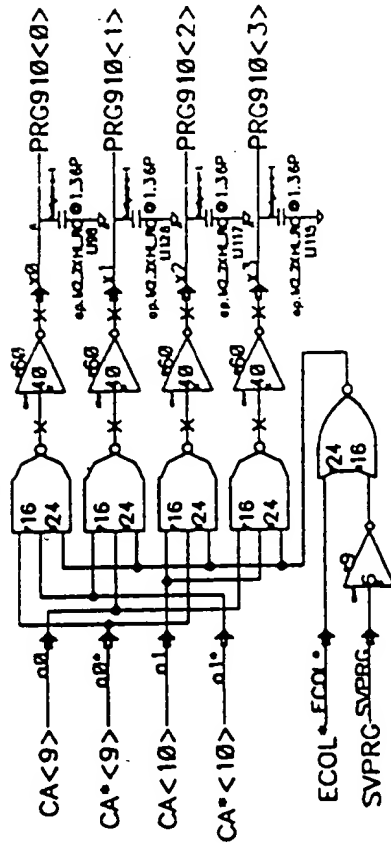


FIGURE 95

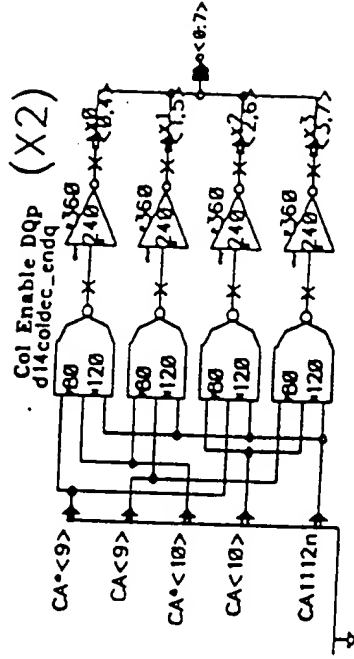


FIGURE 96

## ENCA/SEL8M

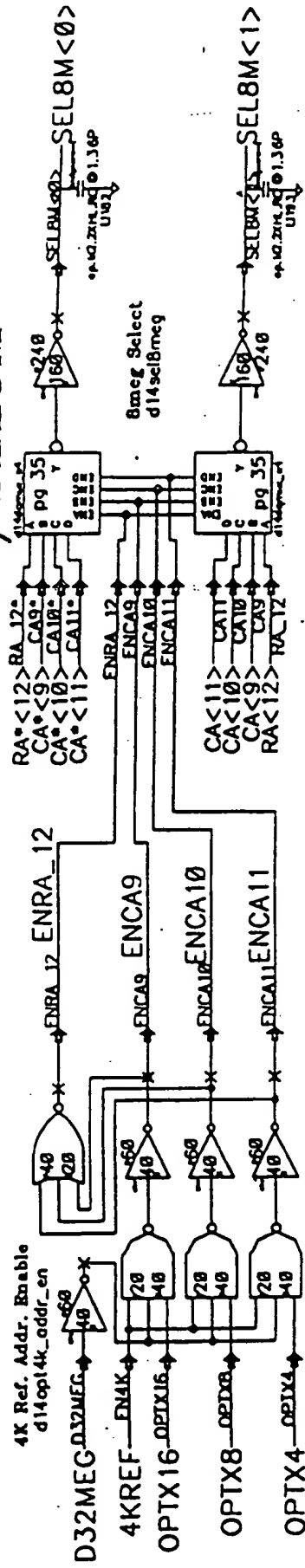


FIGURE 97

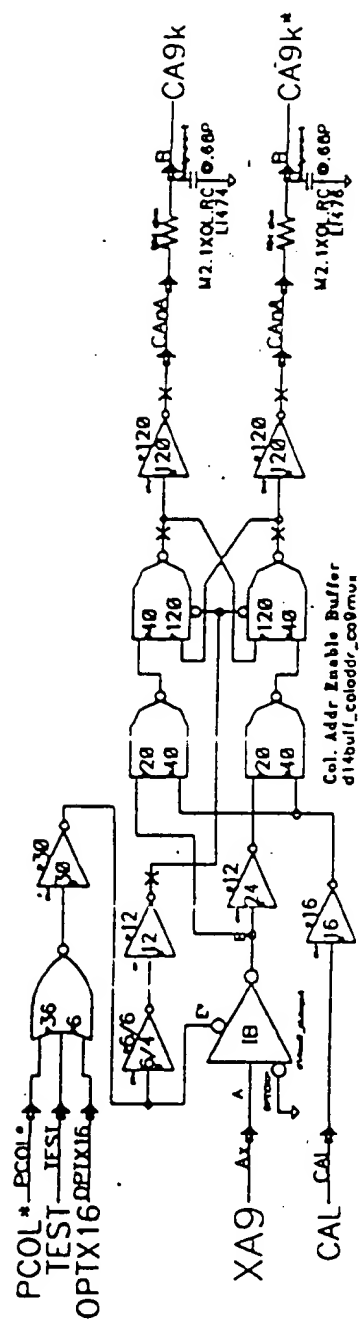


FIGURE 98

## LOCAL ROW DECODE

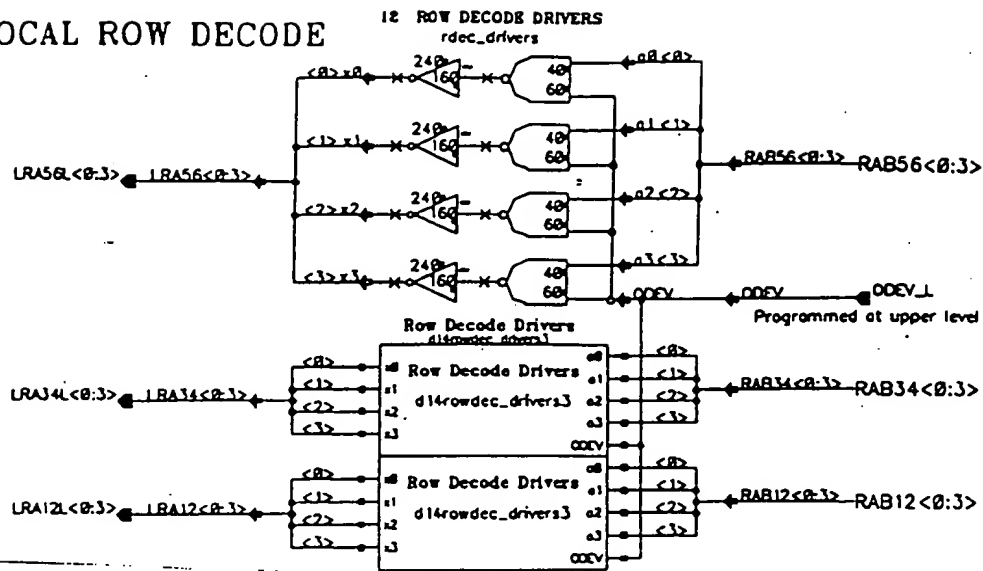


FIGURE 99

## COLUMN SELECT

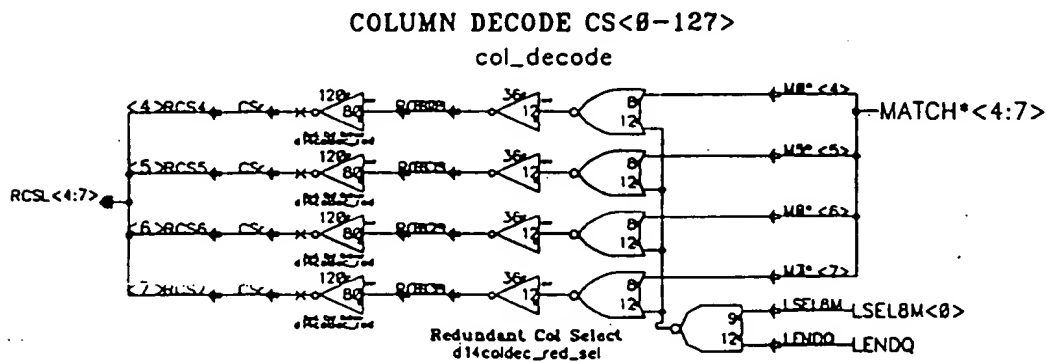


FIGURE 100

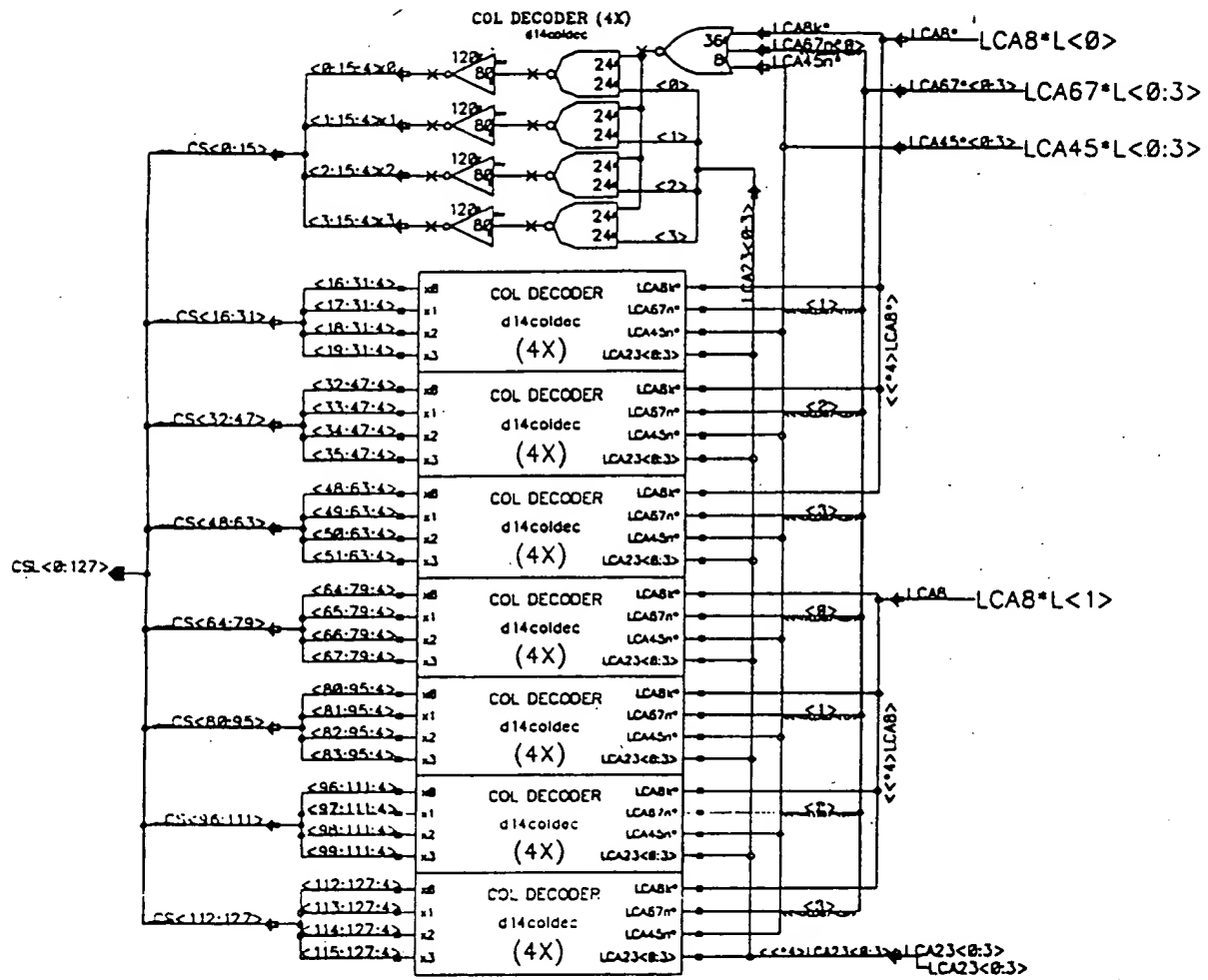


FIGURE 101

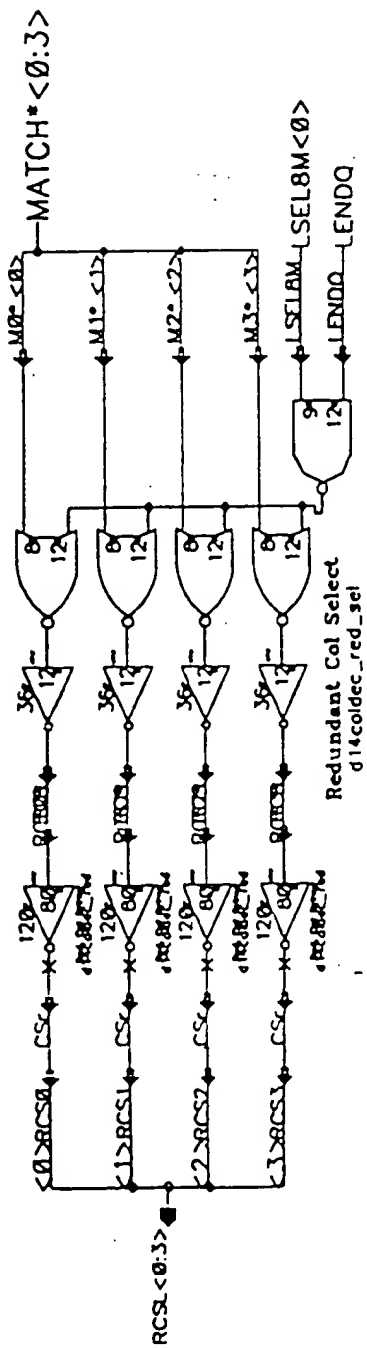
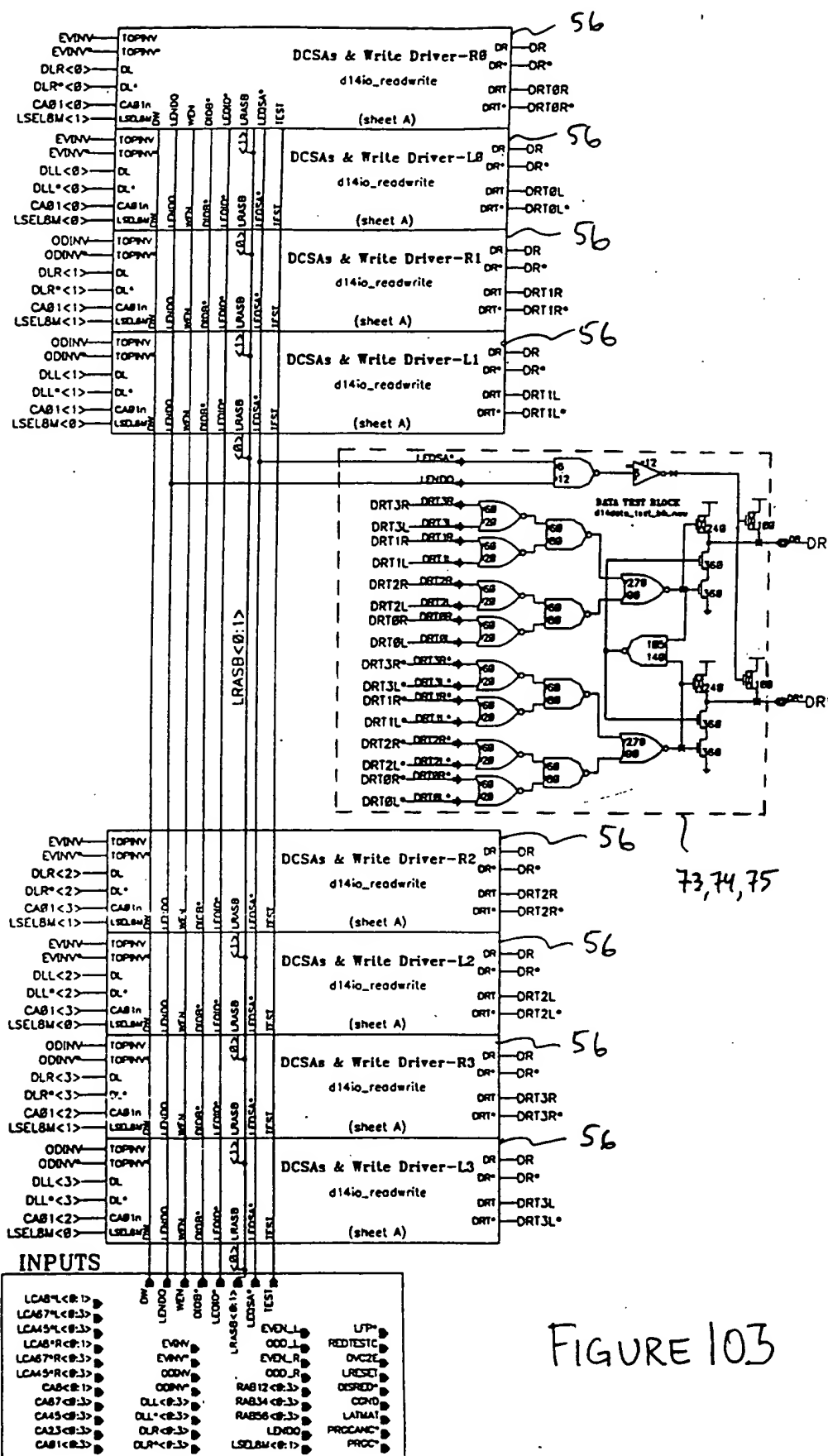
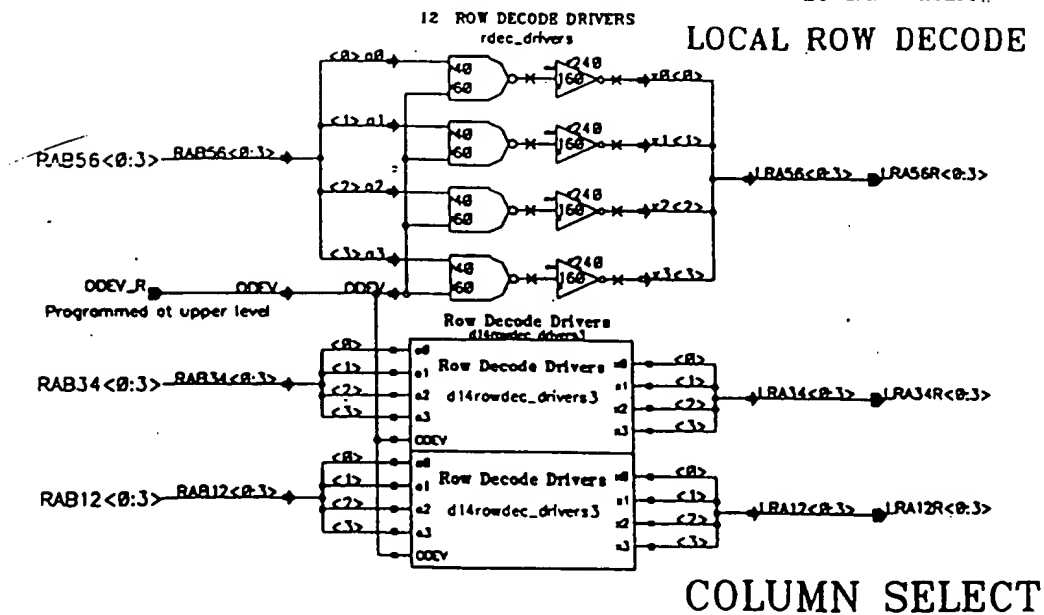
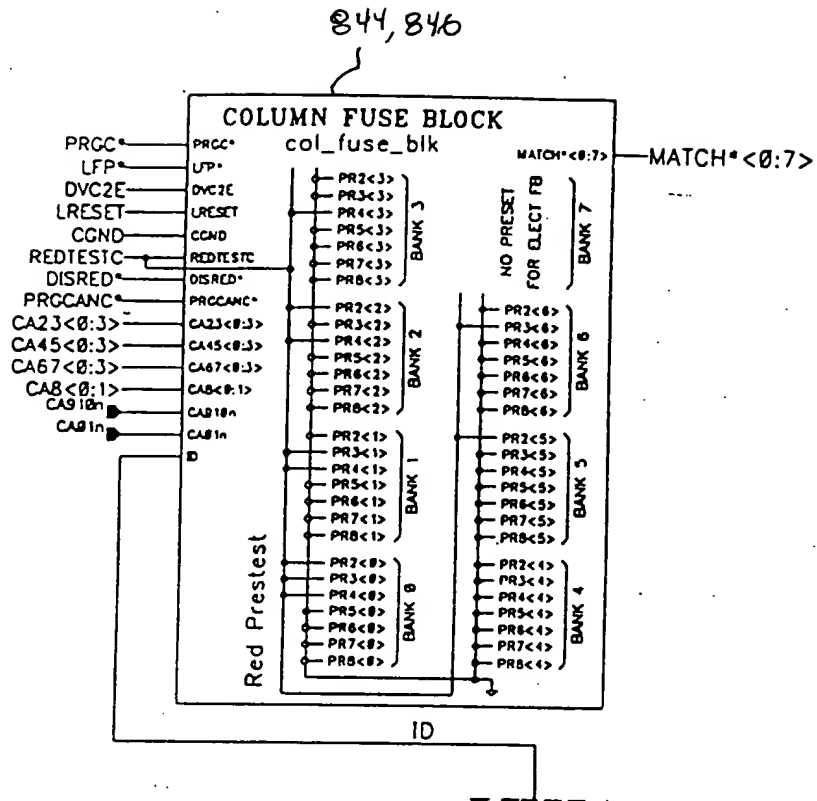


FIGURE 102











# SEVEN LASER FUSE BANKS

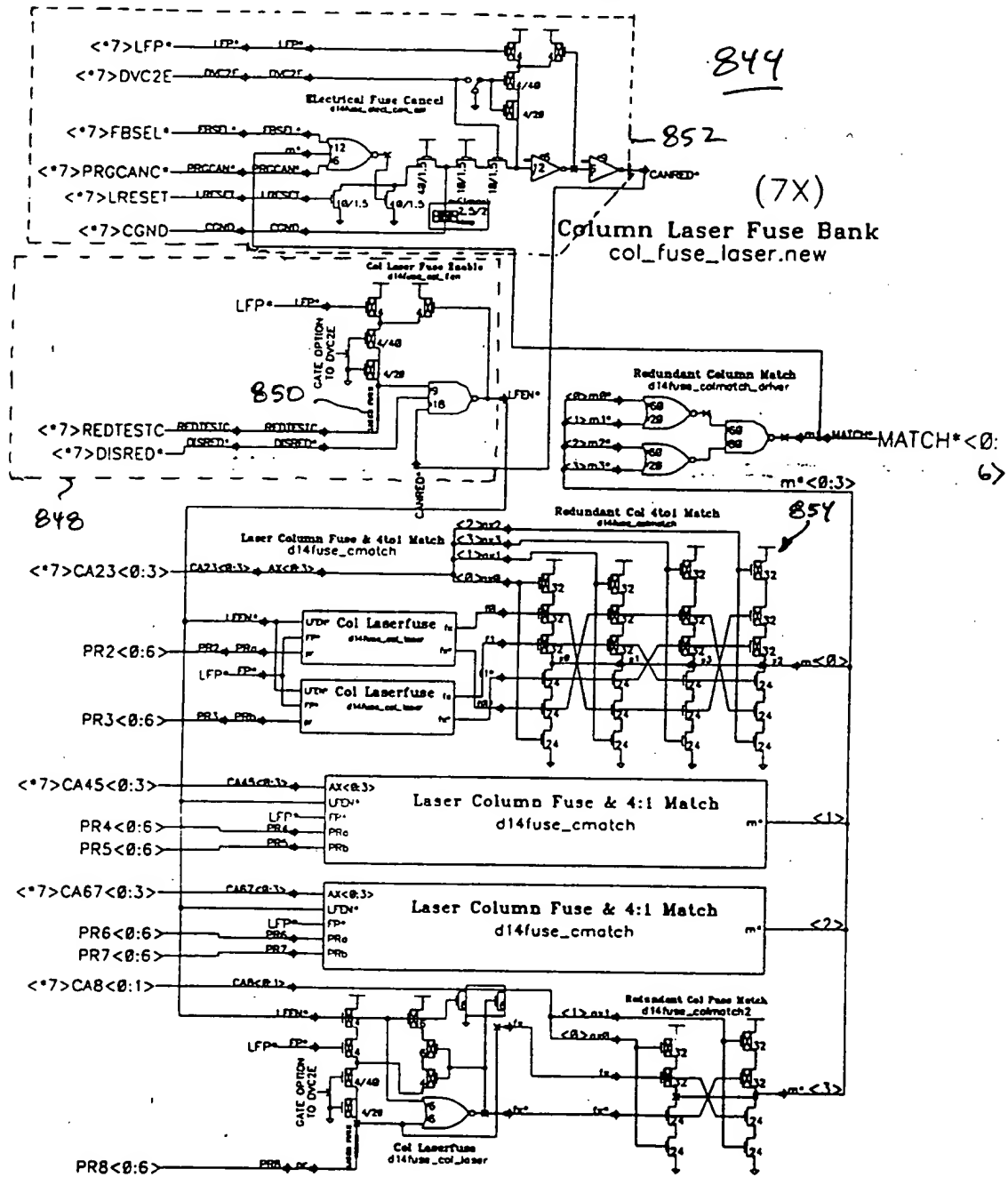


FIGURE 110

# INPUTS

CA23<0:3>	PR2<0>	PR2<2>	PR2<4>	PR2<6>
CA45<0:3>	PR3<0>	PR3<2>	PR3<4>	PR3<6>
CA67<0:3>	PR4<0>	PR4<2>	PR4<4>	PR4<6>
CAB<0:1>	PR5<0>	PR5<2>	PR5<4>	PR5<6>
CA81n	PR6<0>	PR6<2>	PR6<4>	PR6<6>
CA918n	PR7<0>	PR7<2>	PR7<4>	PR7<6>
LTP*	PR8<0>	PR8<2>	PR8<4>	PR8<6>
DVC2C				
LRESET	PR2<1>	PR2<3>	PR2<5>	
COND	PR3<1>	PR3<3>	PR3<5>	
REDTESTC	PR4<1>	PR4<3>	PR4<5>	
DISRED*	PR5<1>	PR5<3>	PR5<5>	
PRCCANC*	PR6<1>	PR6<3>	PR6<5>	
PRCC*	PR7<1>	PR7<3>	PR7<5>	
ID	PR8<1>	PR8<3>	PR8<5>	

FIGURE 111

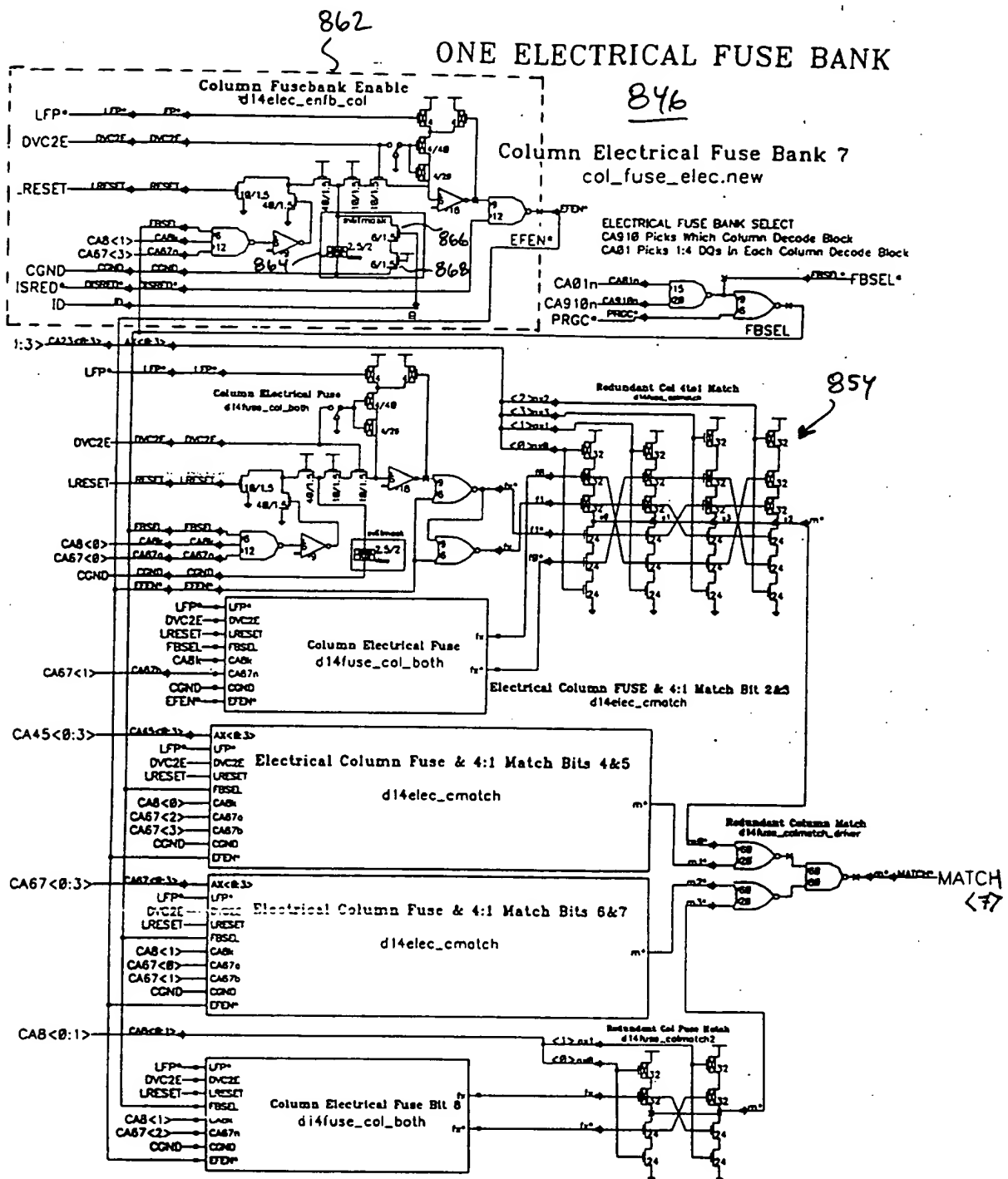


FIGURE 112

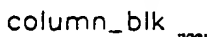


FIGURE 113

# INPUTS FROM PERIPH.

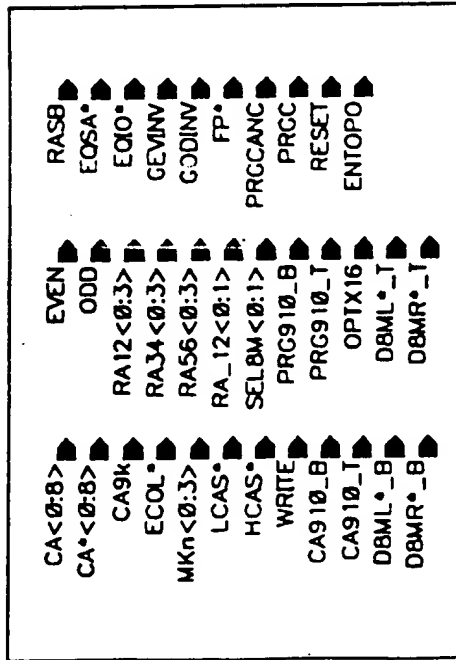


FIGURE 114

# OUTPUTS TO COLUMN BLOCK

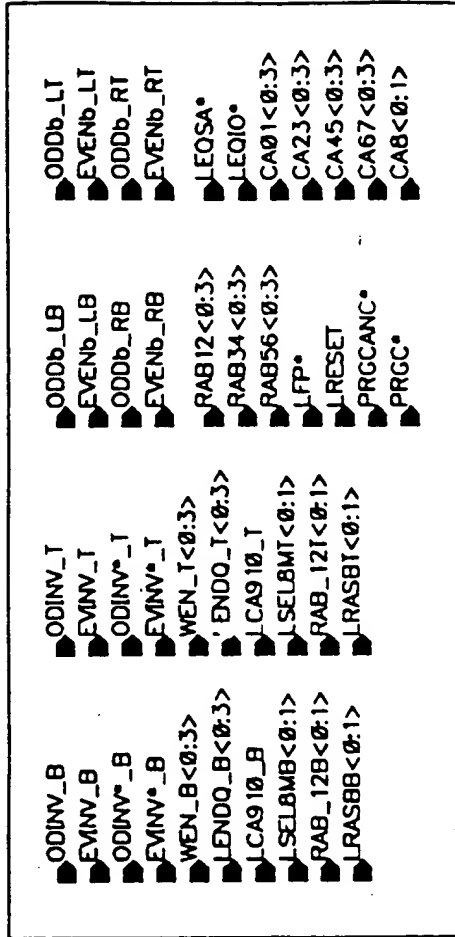


FIGURE 115

# SIGNALS PASSING THROUGH

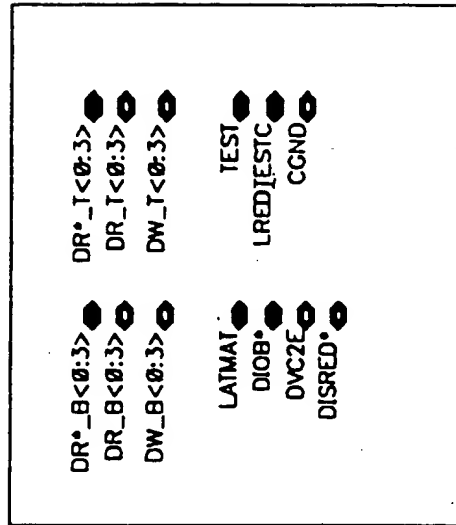


FIGURE 116

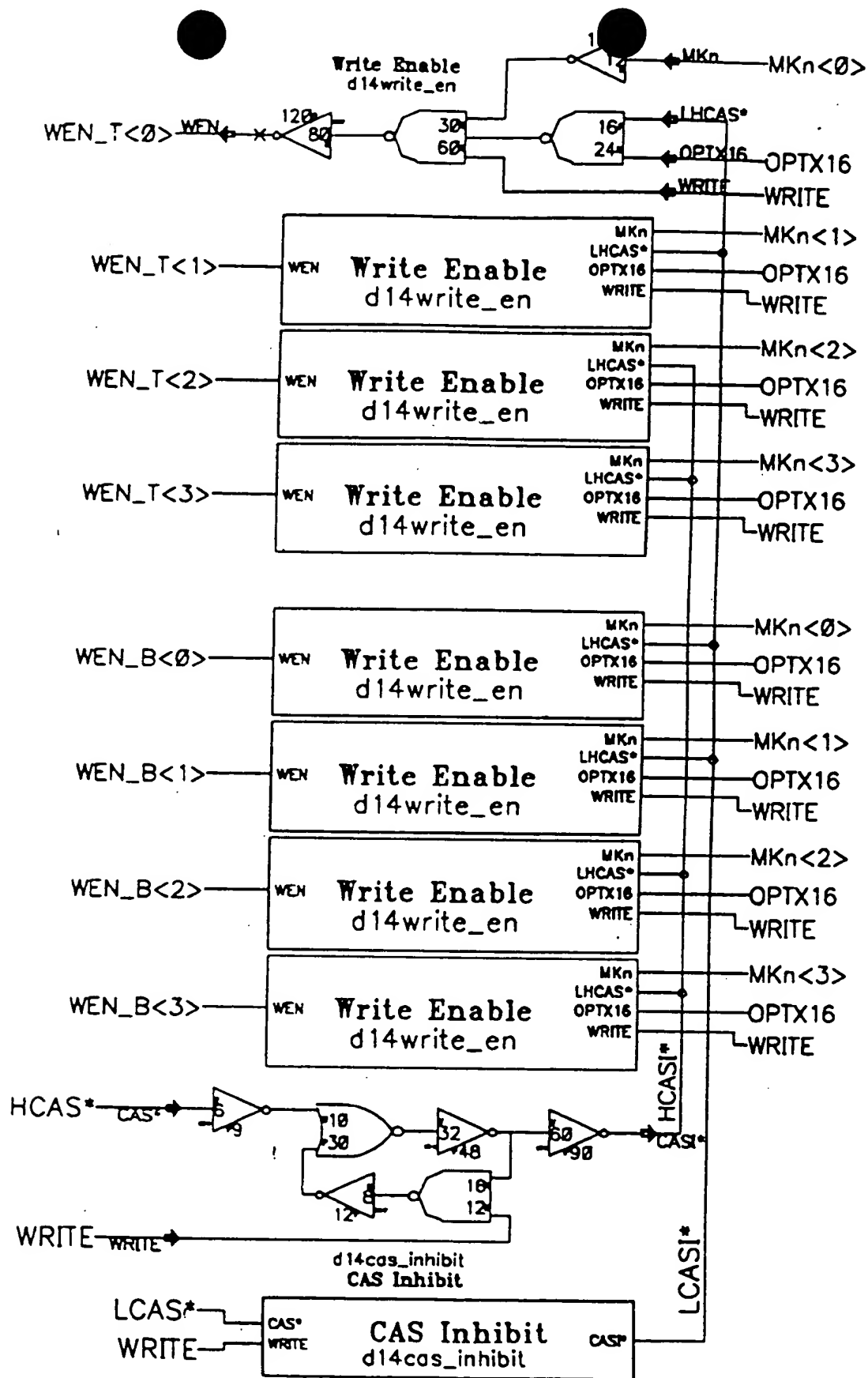


FIGURE 117

# INPUTS FROM BOTTOM ROW RED.

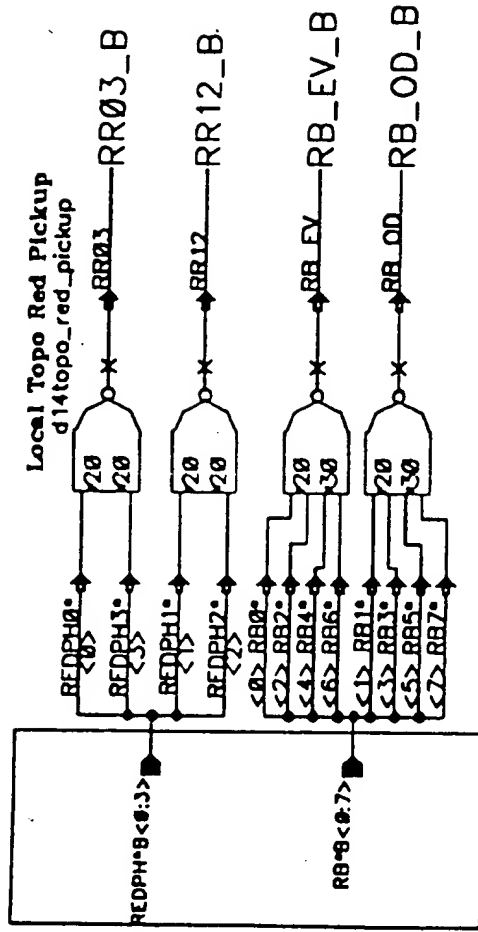


FIGURE 118

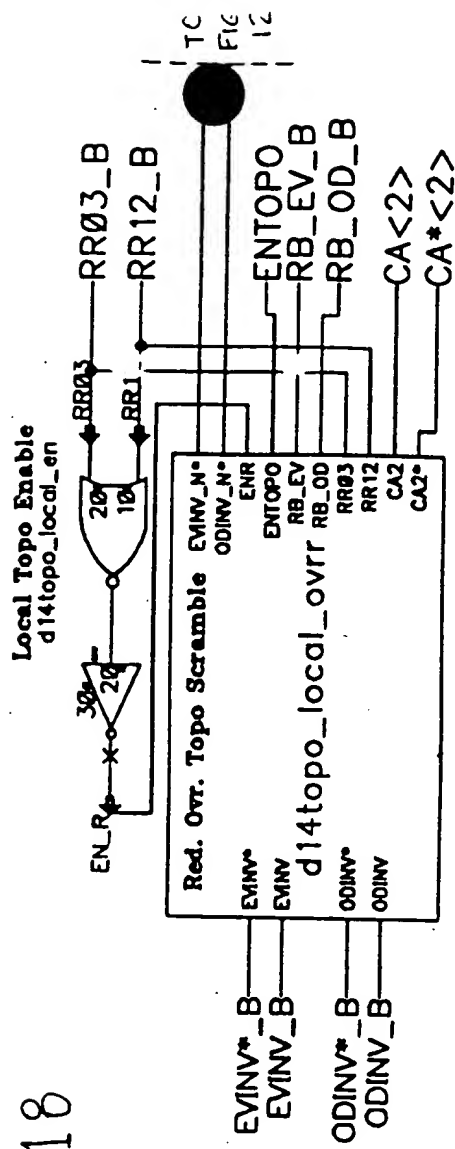


FIGURE 119



222

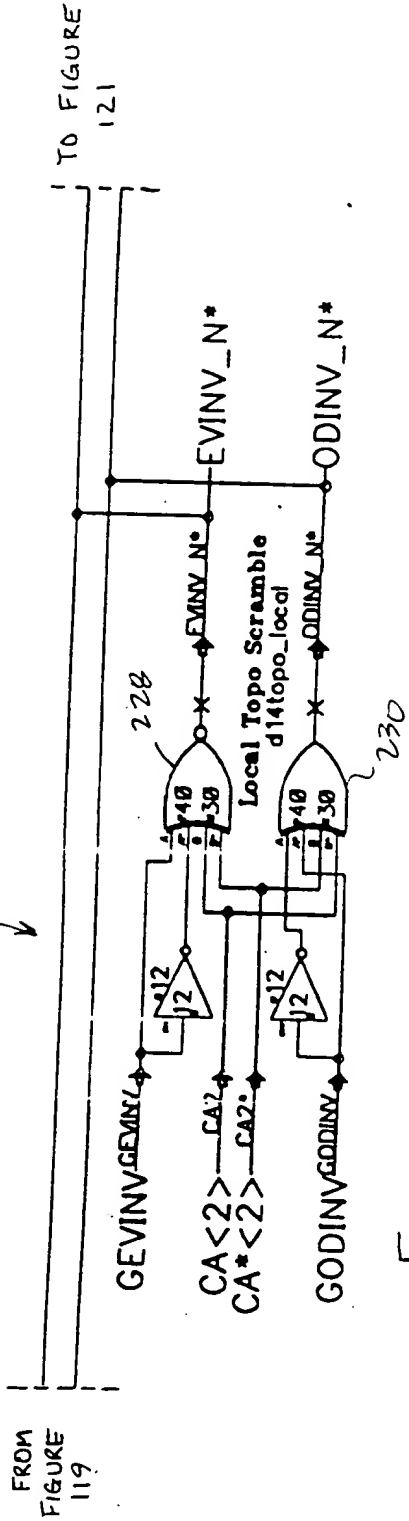


FIGURE 120

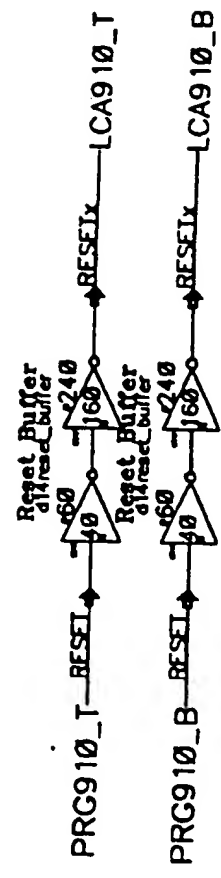


FIGURE 122

FROM  
FIGURE  
120

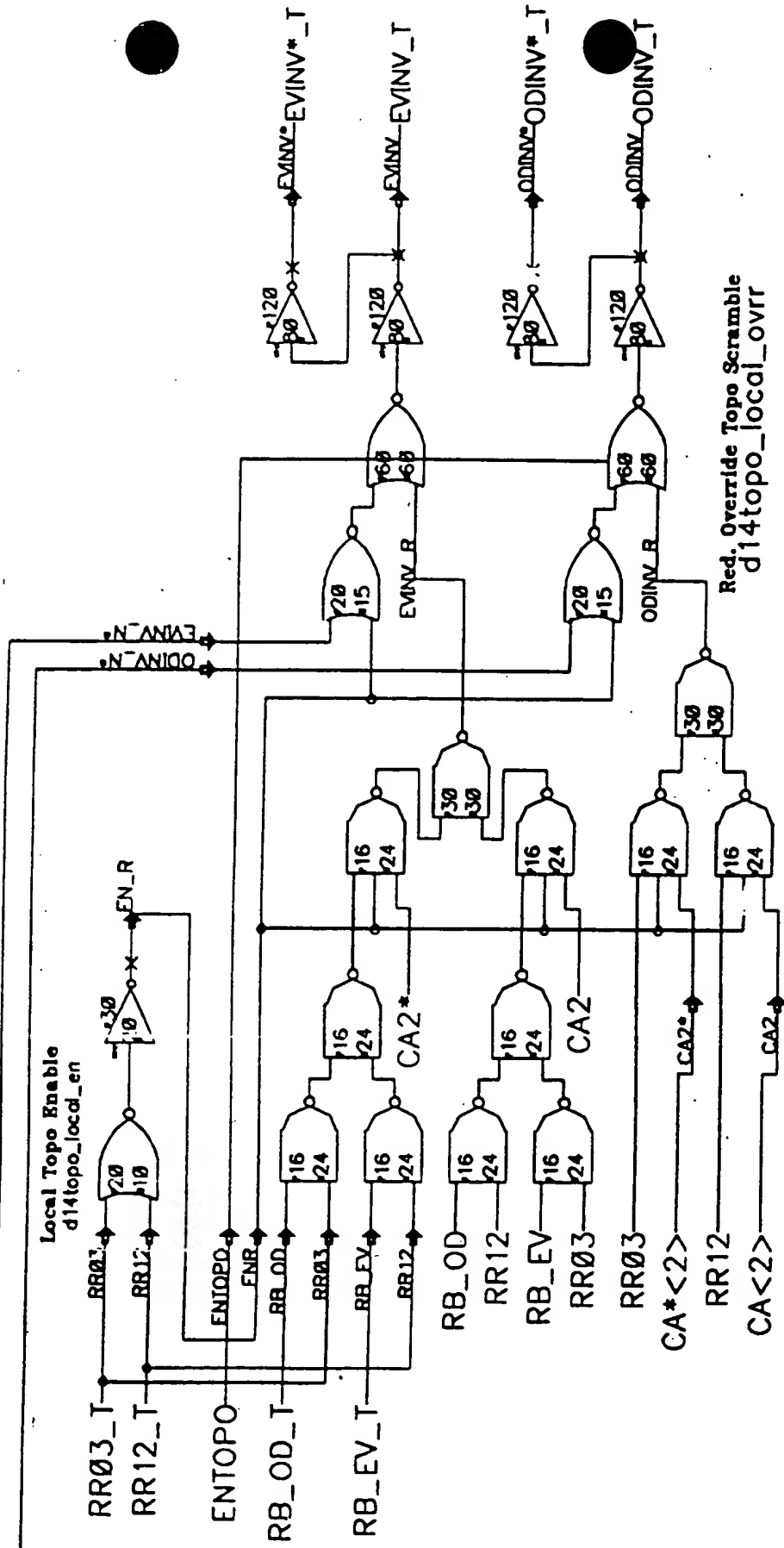


FIGURE 121

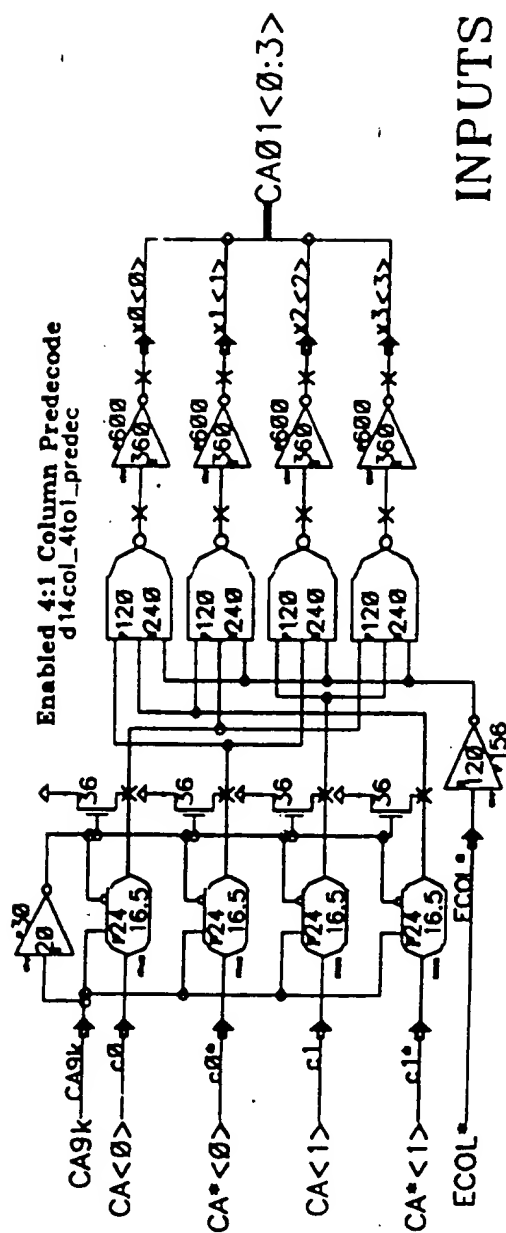


FIGURE 123

INPUTS FROM TOP ROW RED.

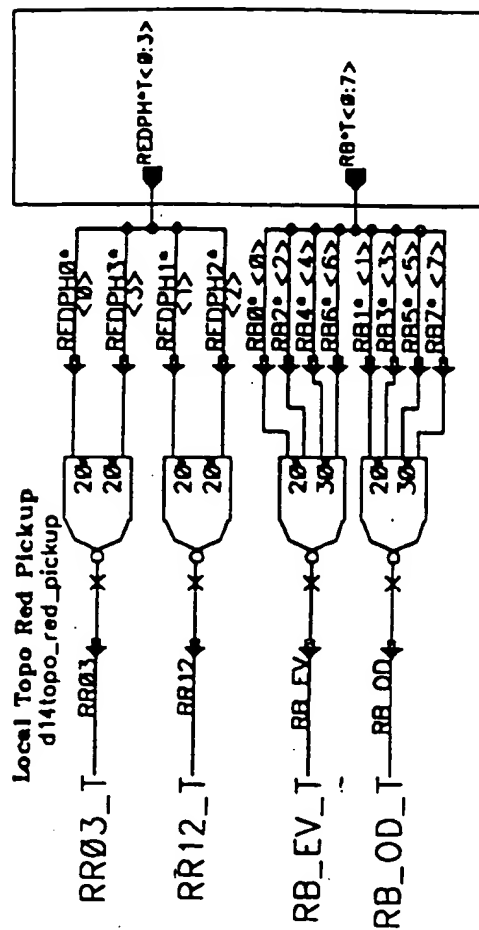


FIGURE 124

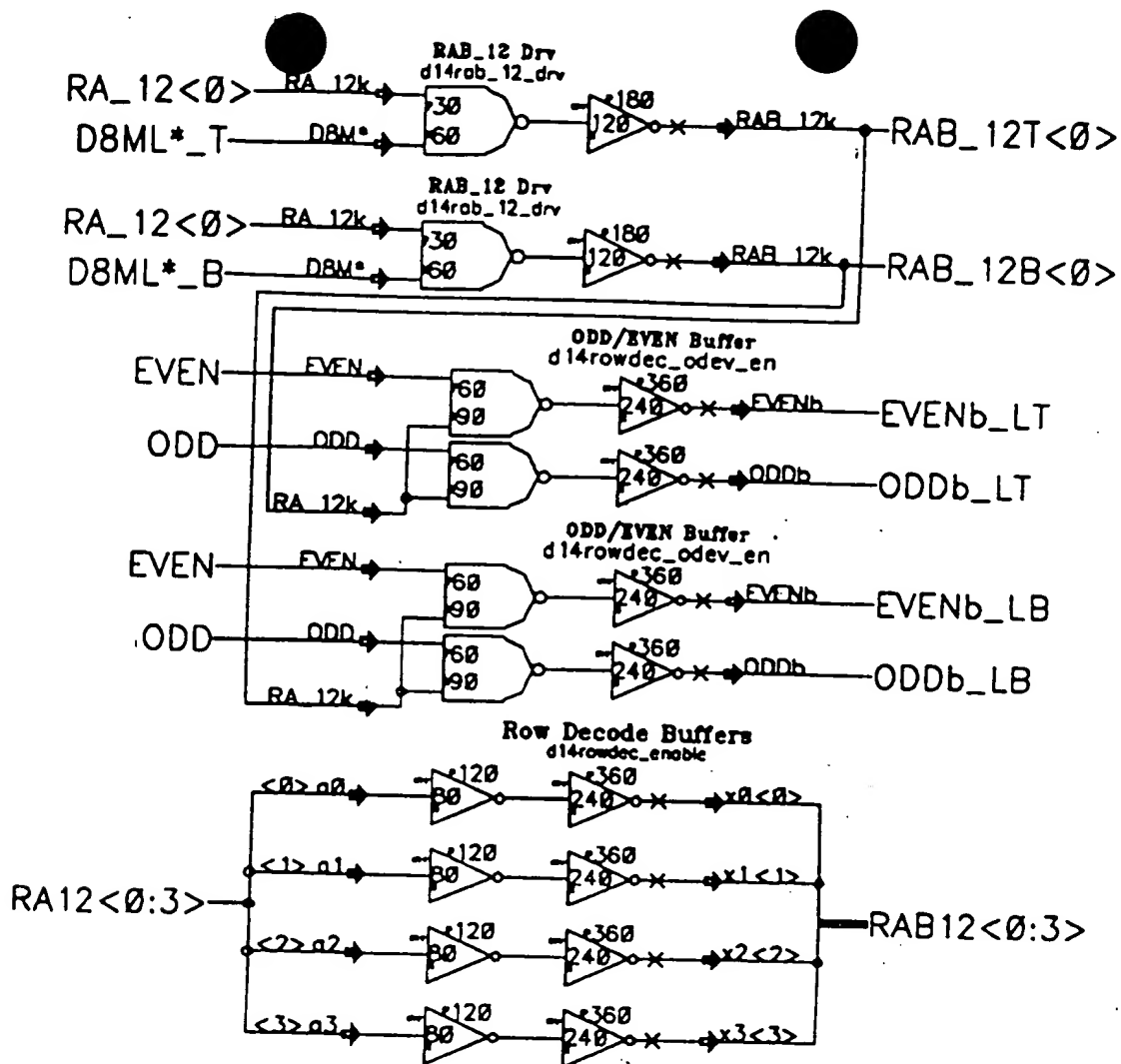


FIGURE 125

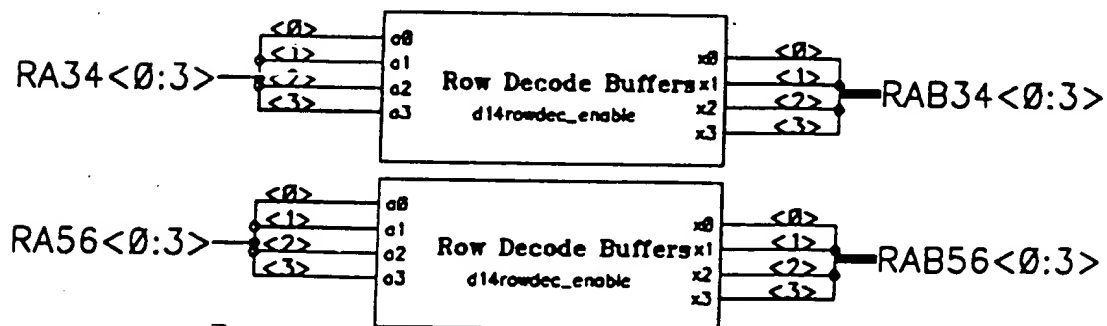


FIGURE 126

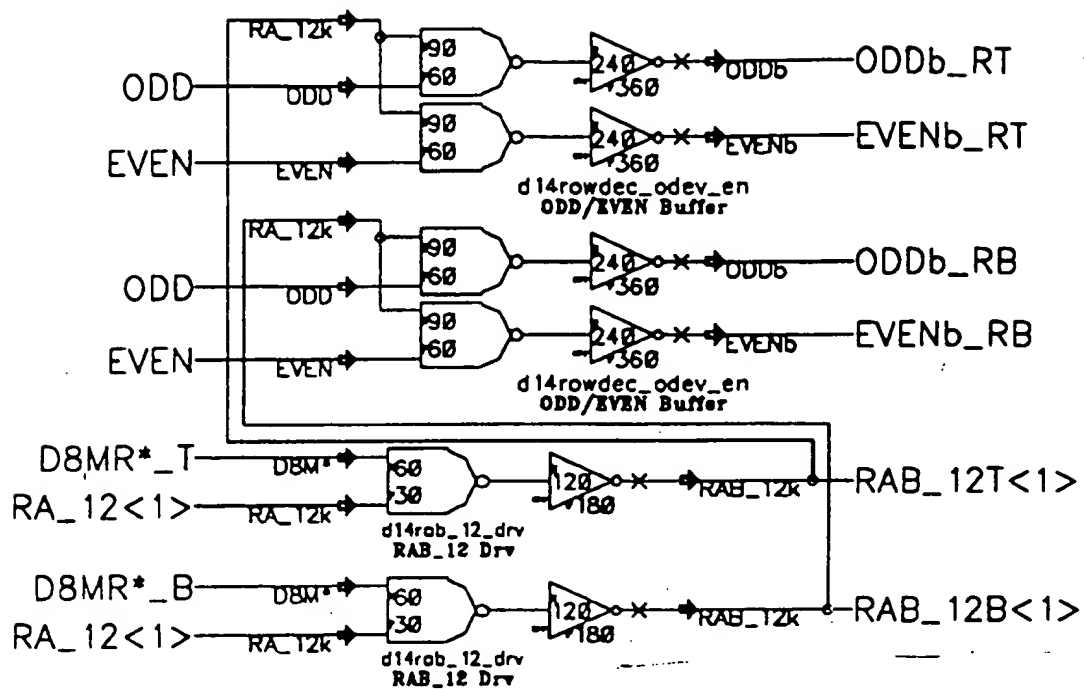


FIGURE 127

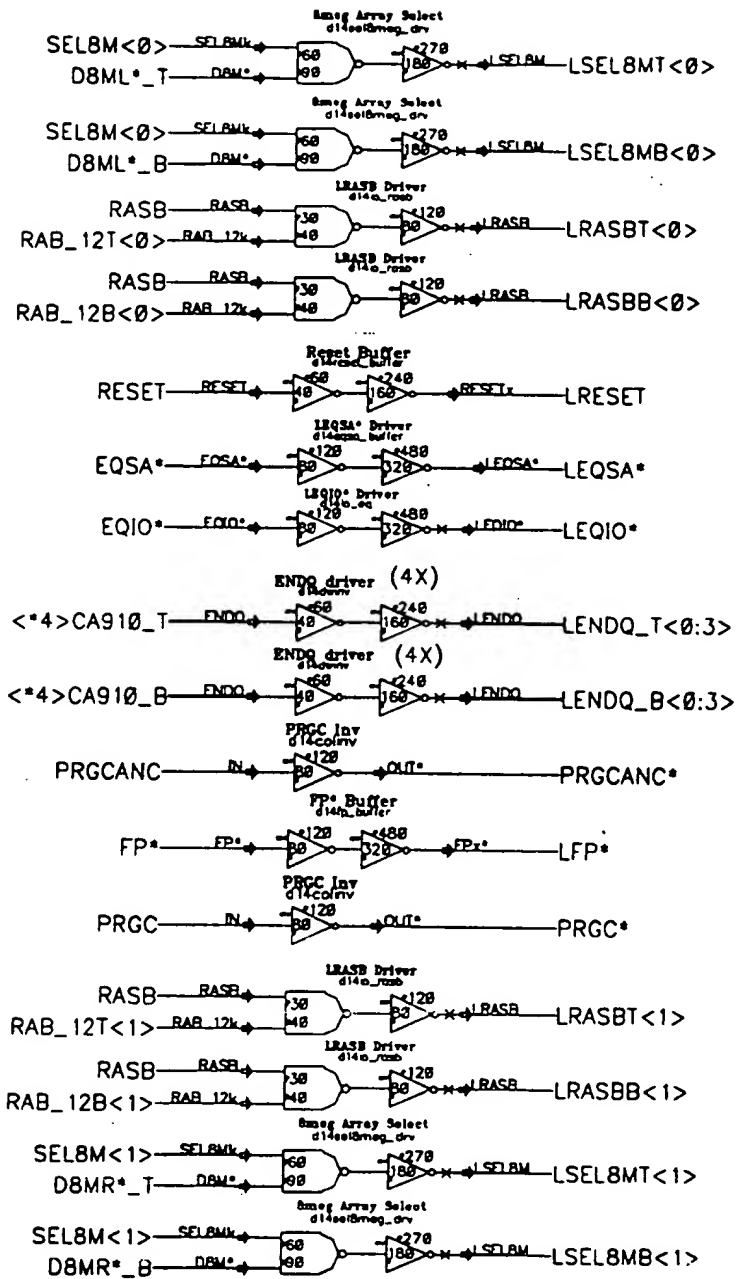


FIGURE 128

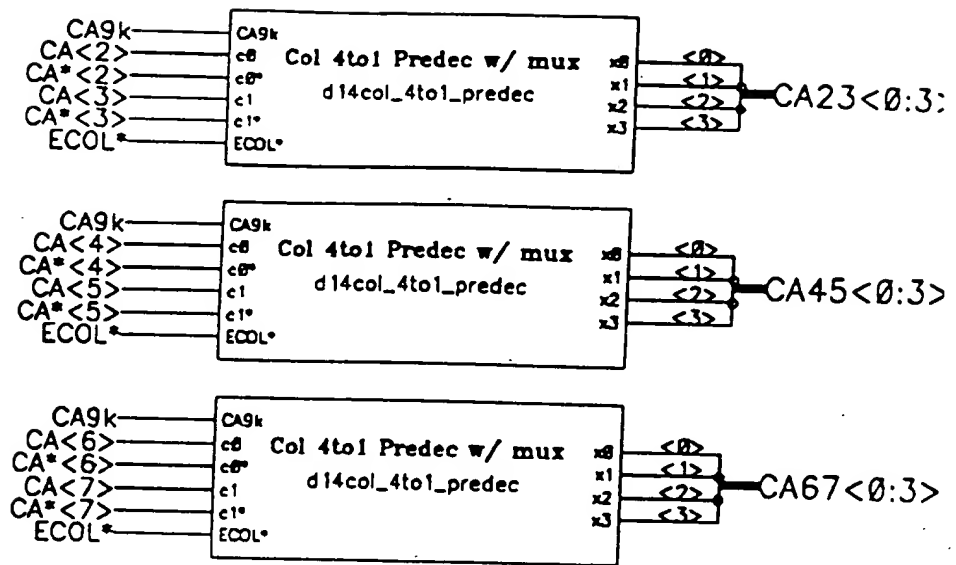


FIGURE 129

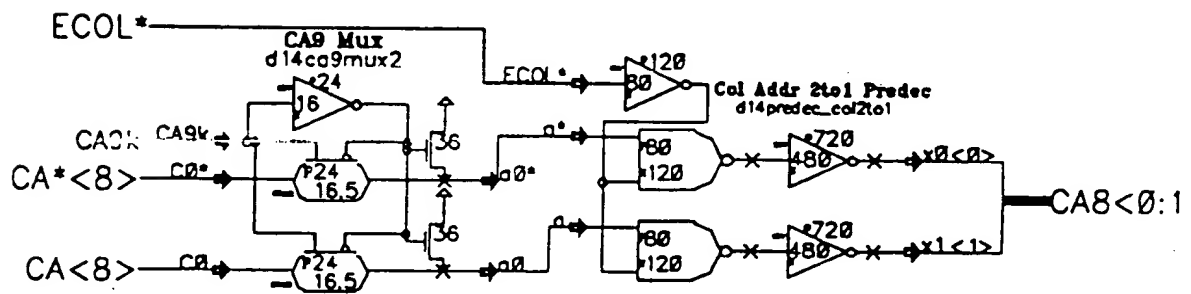

















FIGURE 130

# INPUTS

ISO\* <0:1>   
 EQ   
 ENPH\* <0:1>   
 ENSA\*   
 EPSA\*   
 RPRE   
 RBPPE   
 REDTESTC   
 PRG910 <1,2>   
 PRGCANR   
 DBML\*\_T   
 DBMR\*\_T   
 DBML\*\_B   
 DBMR\*\_B   
 POWERUP\* 

# OUTPUTS

























ISO_L 	DBML_T <0:1> 
EQ*_L 	DBMR_T <0:1> 
ENPH_L 	P8MbLT 
ENSA_L 	P8MbRT 
EPSA_L 	
RPRE*_L 	DBML_B <0:1> 
RBPPE*_L 	DBMR_B <0:1> 
	P8MbLB 
ISO_R 	P8MbRB 
EQ*_R 	
ENPH_R 	
ENSA_R 	
EPSA_R 	
RPRE*_R 	
RBPPE*_R 	
LREDTESTC 	
LPRGCANR <1,2> 	

FIGURE 131



# RIGHTSIDE OF PERIPH GAP

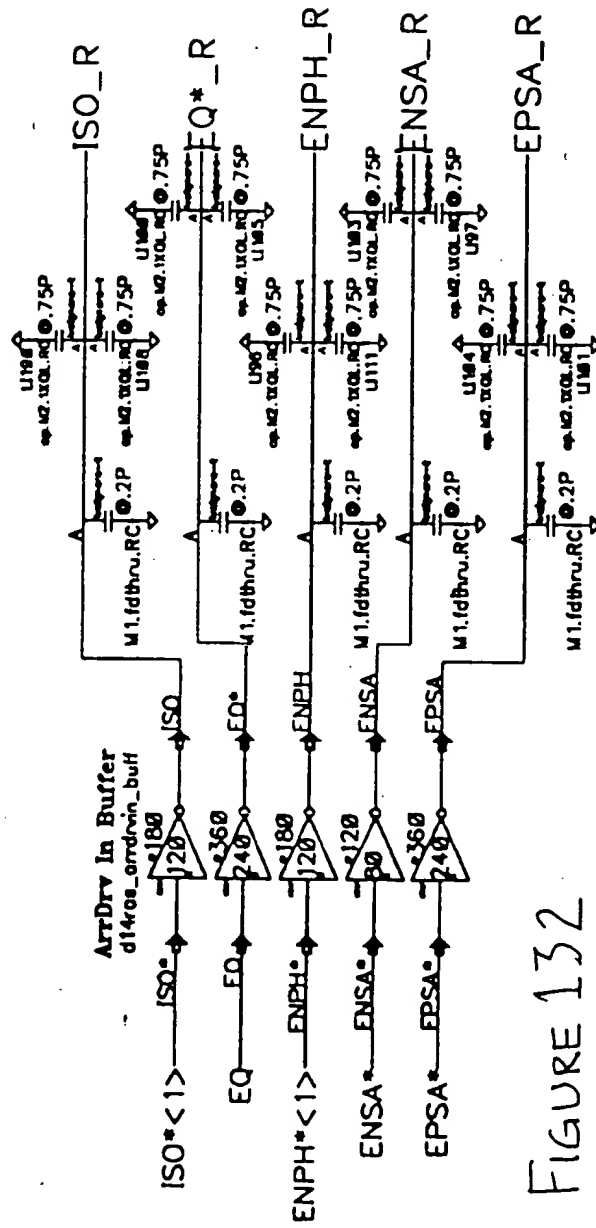


FIGURE 132

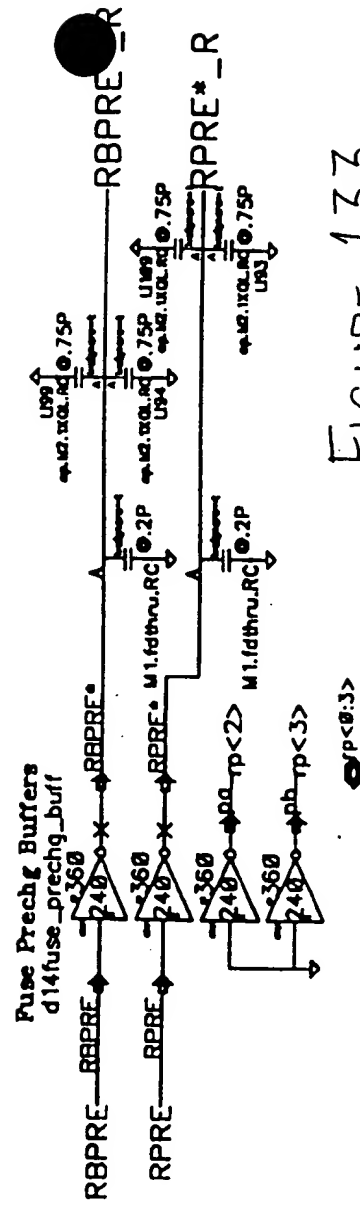


FIGURE 133

# LEFTSIDE OF PERIPH GAP

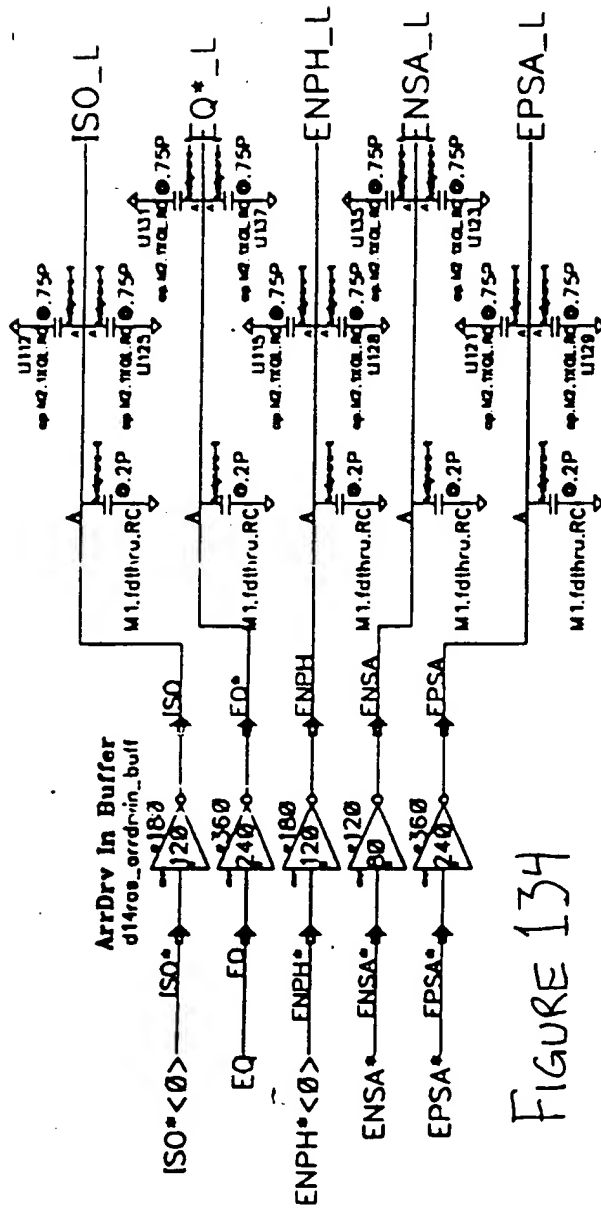


FIGURE 134

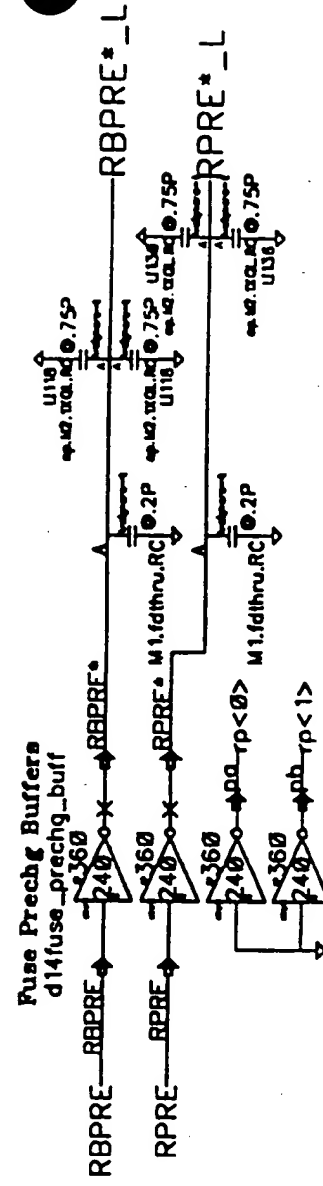


FIGURE 135

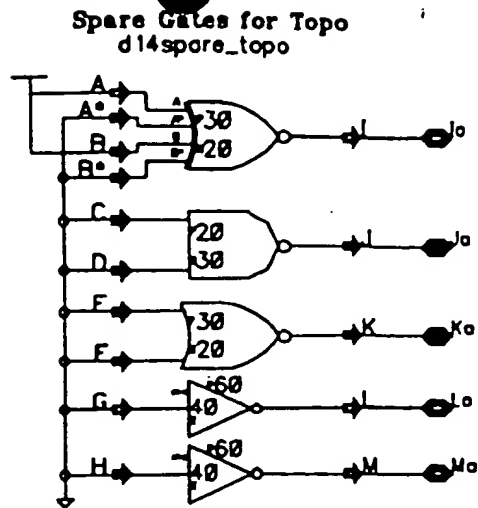


FIGURE 136

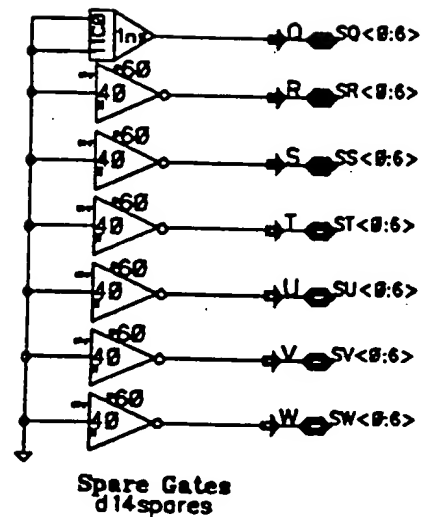


FIGURE 137

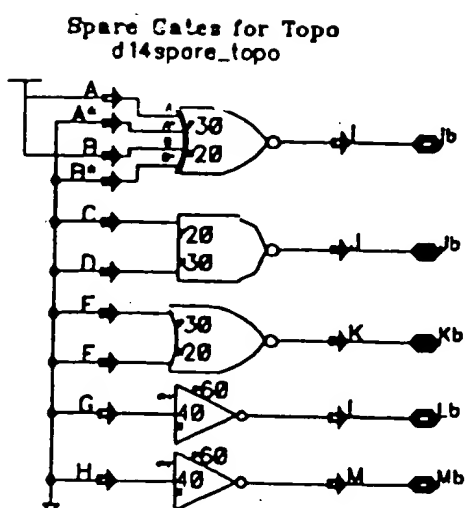


FIGURE 138

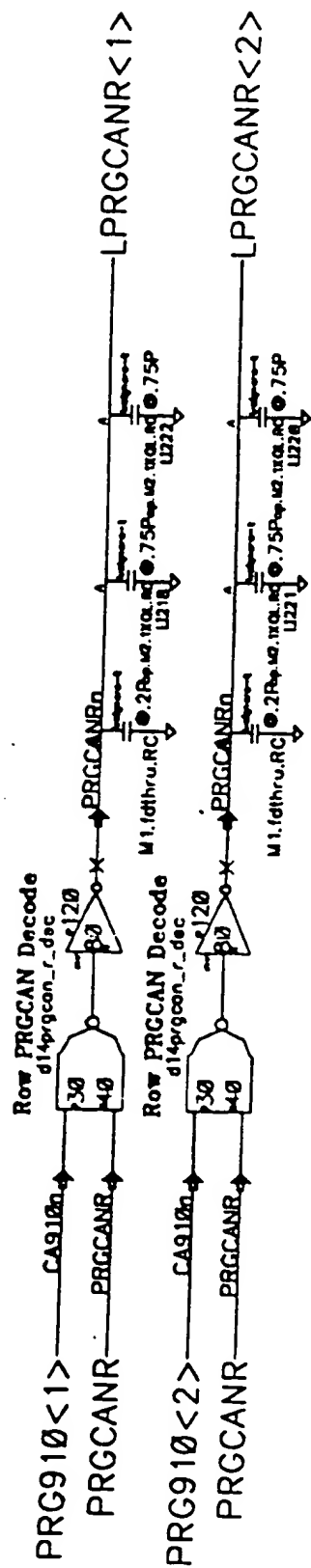


FIGURE 139

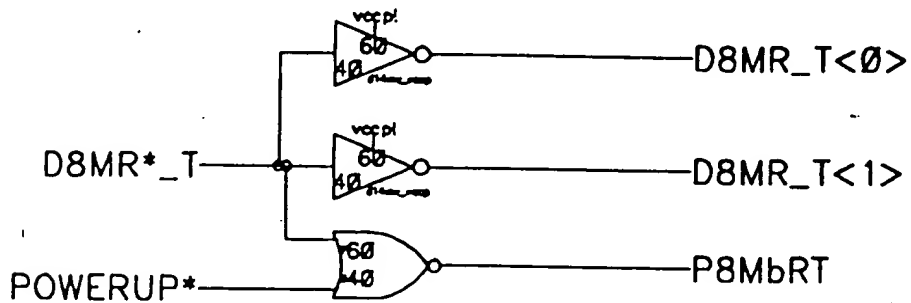
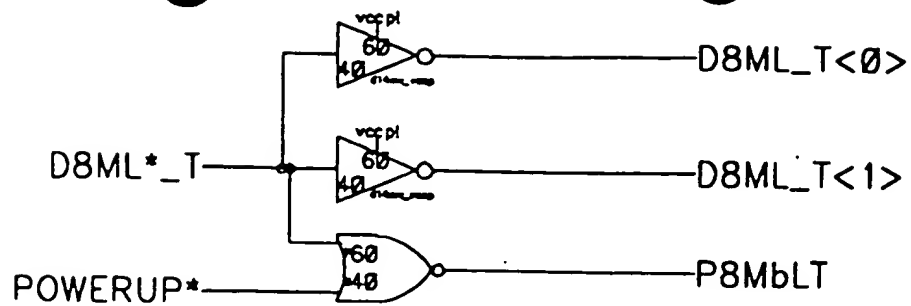


FIGURE 140

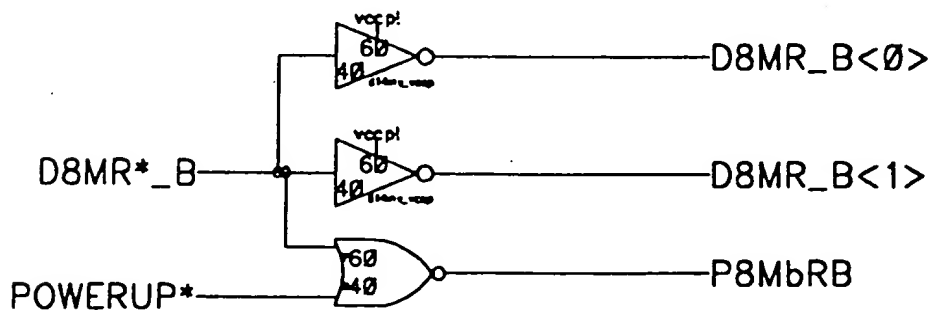
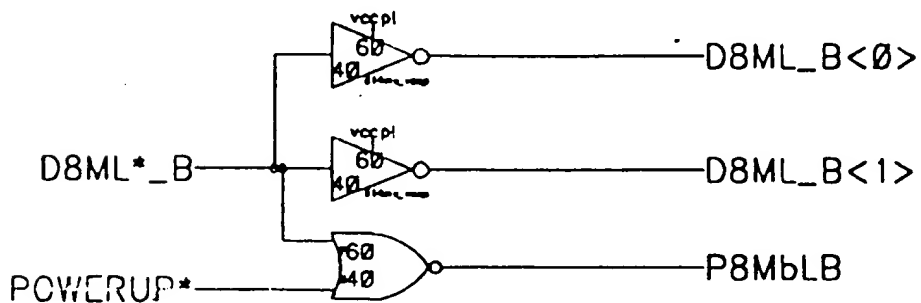


FIGURE 141

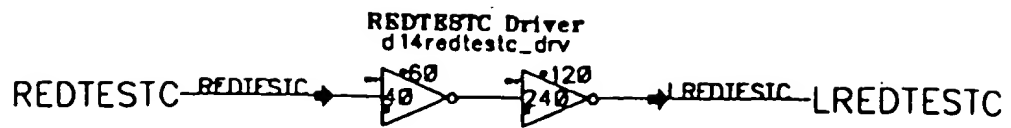
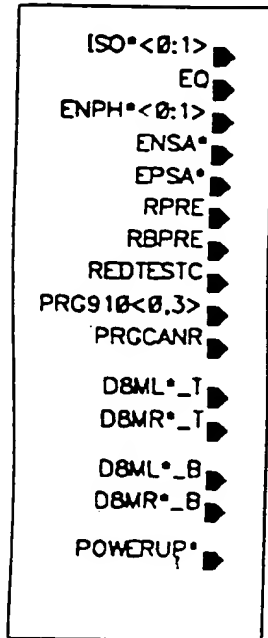


FIGURE 142

# INPUTS



# OUTPUTS

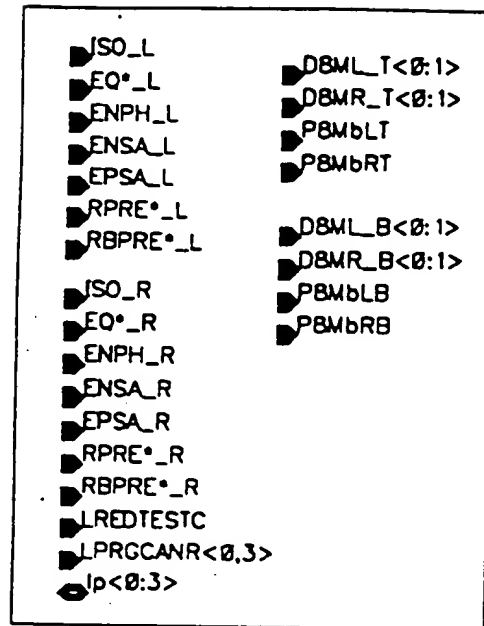


FIGURE 143

# LEFTSIDE OF PERIPH GAP

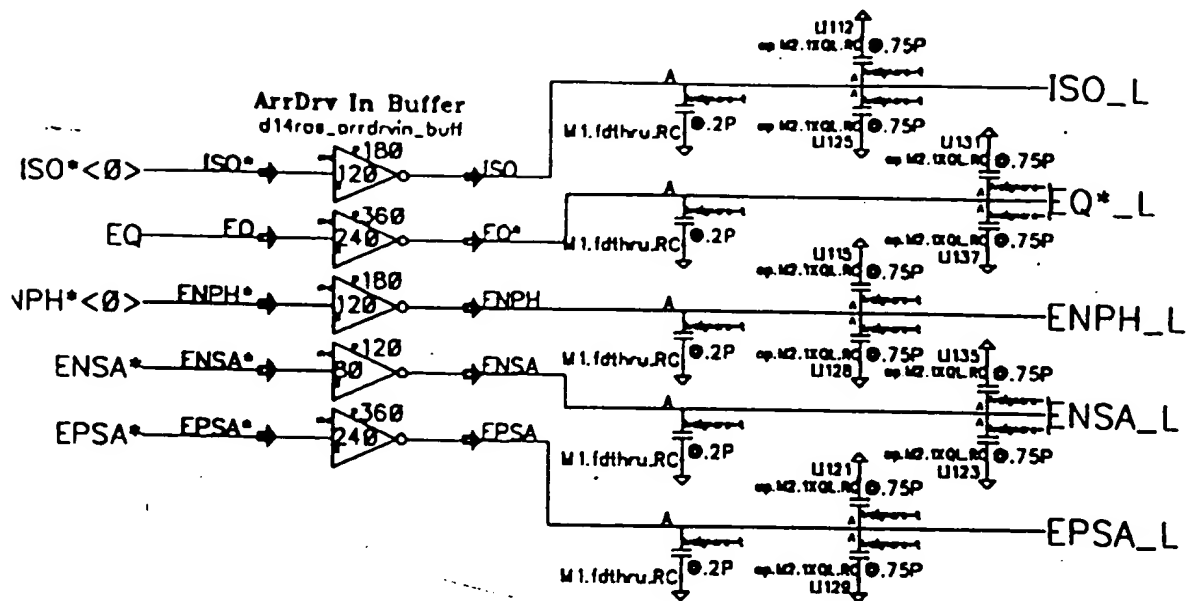


FIGURE 144

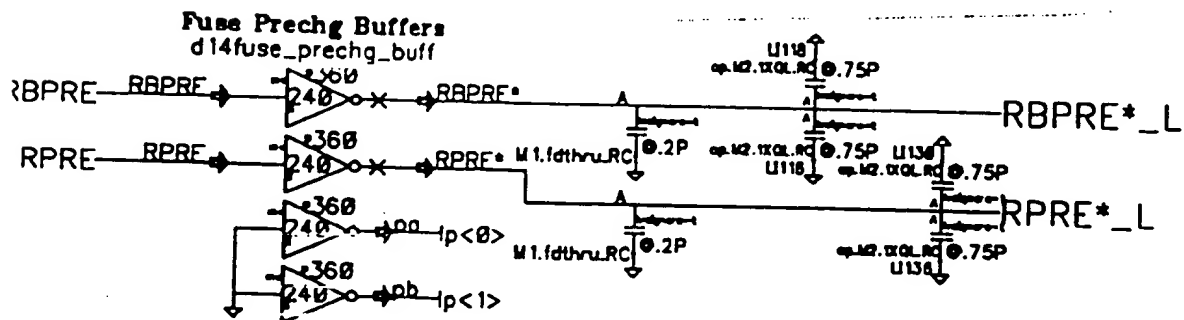


FIGURE 145



# RIGHTSIDE OF PERIPH GAP

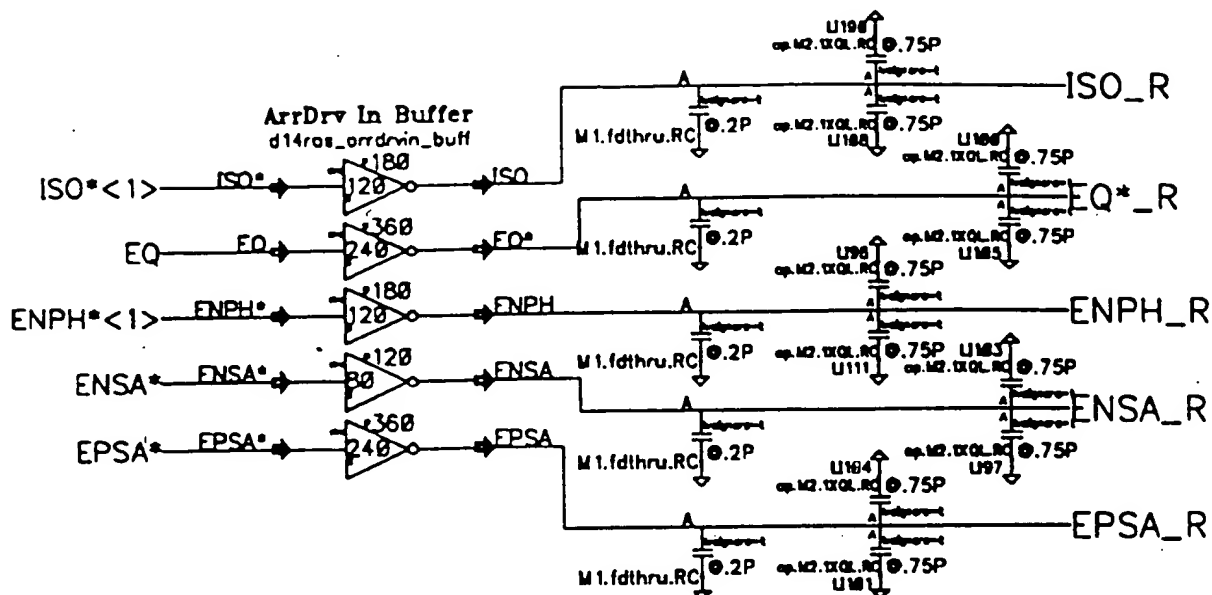


FIGURE 146

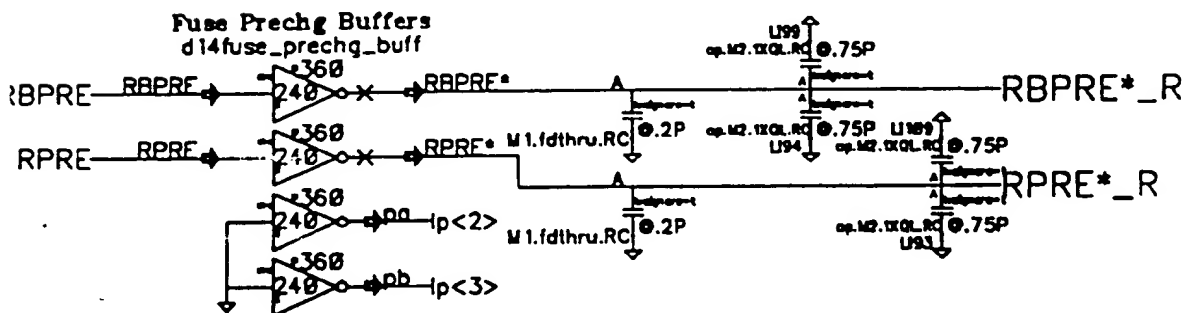


FIGURE 147

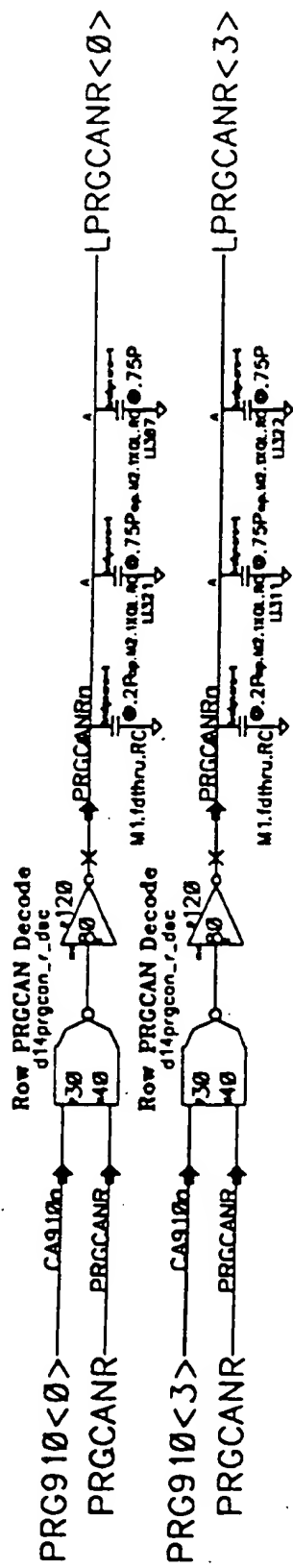


FIGURE 148

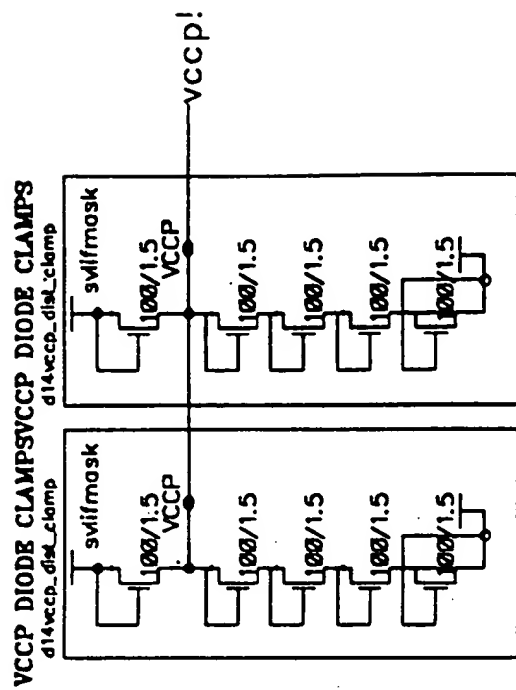


FIGURE 149

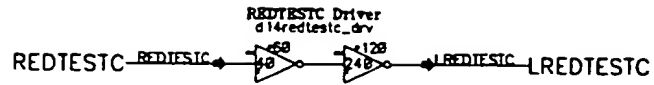


FIGURE 150

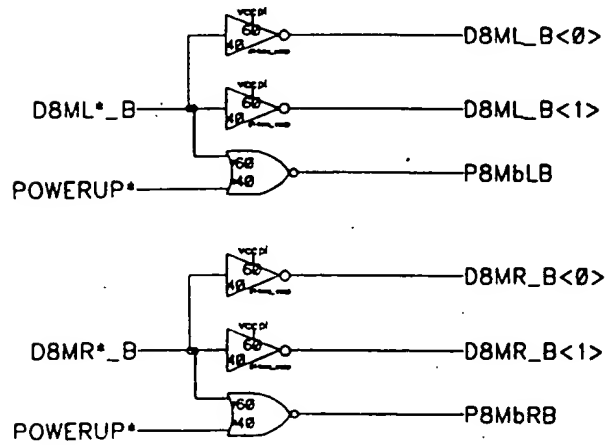


FIGURE 151

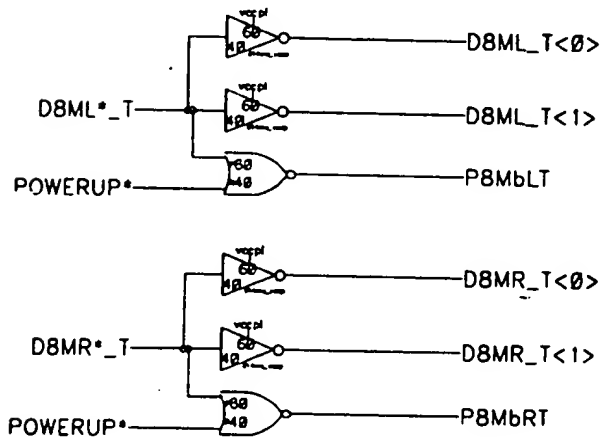
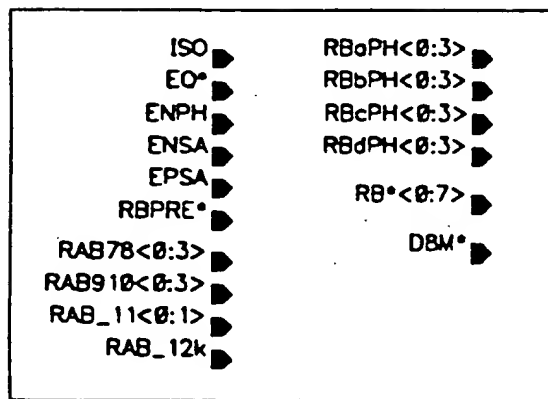


FIGURE 152

# INPUTS



# I/O

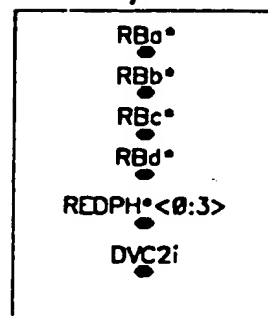


FIGURE 153

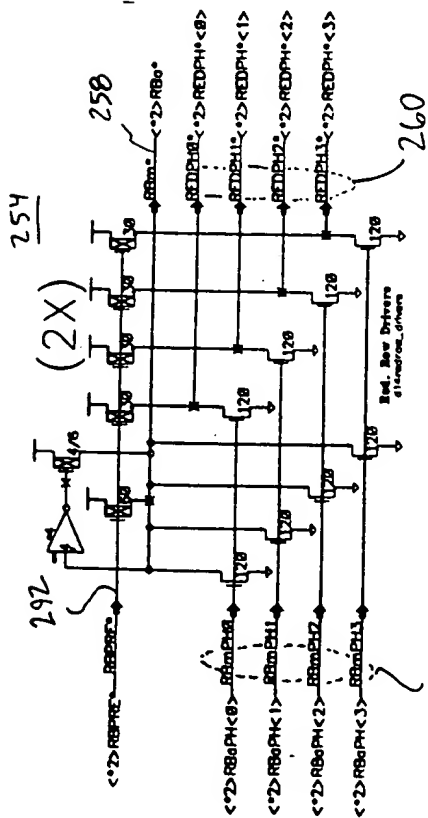


FIGURE 154

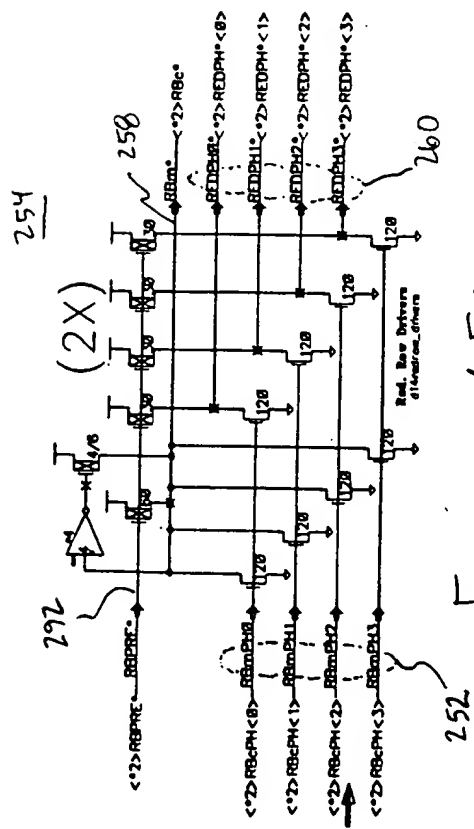


FIGURE 156

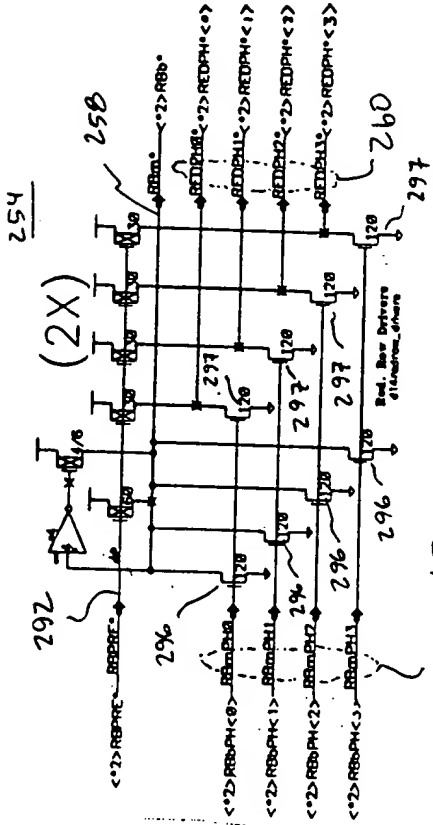


FIGURE 155

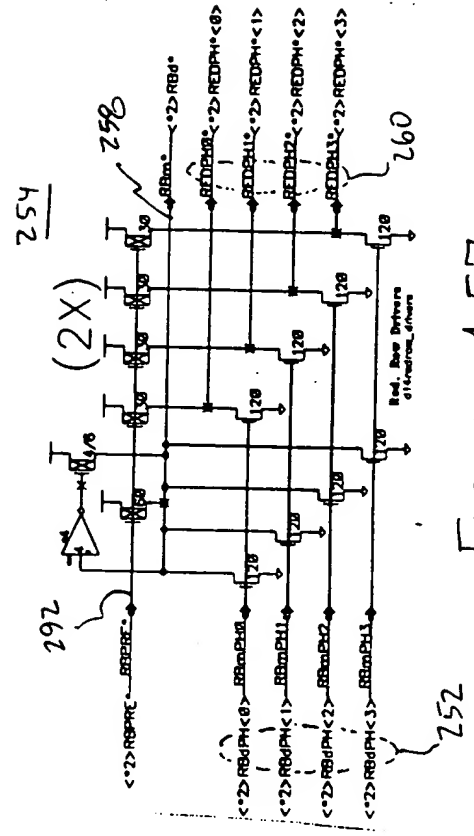


FIGURE 157

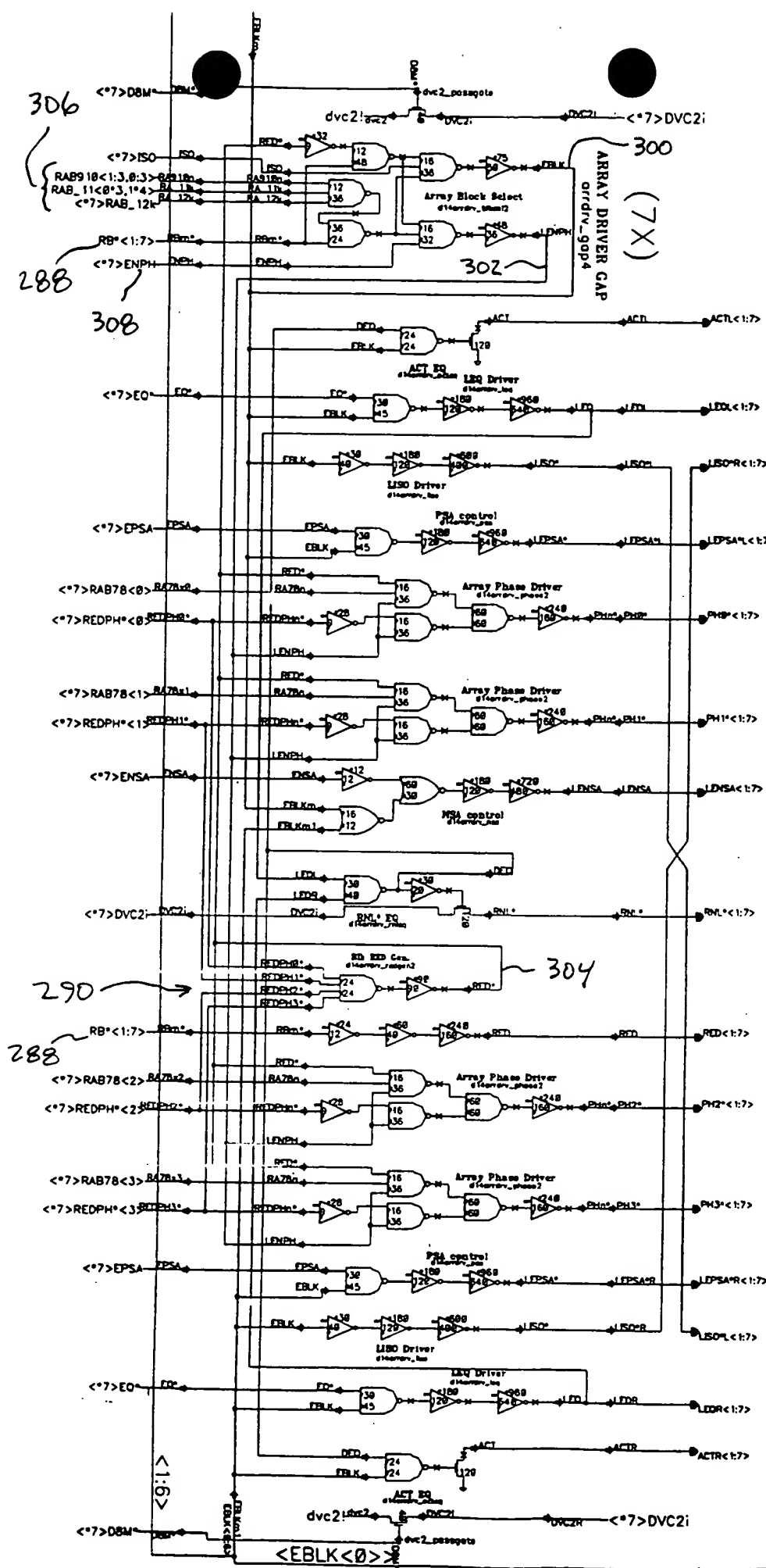


FIGURE  
158

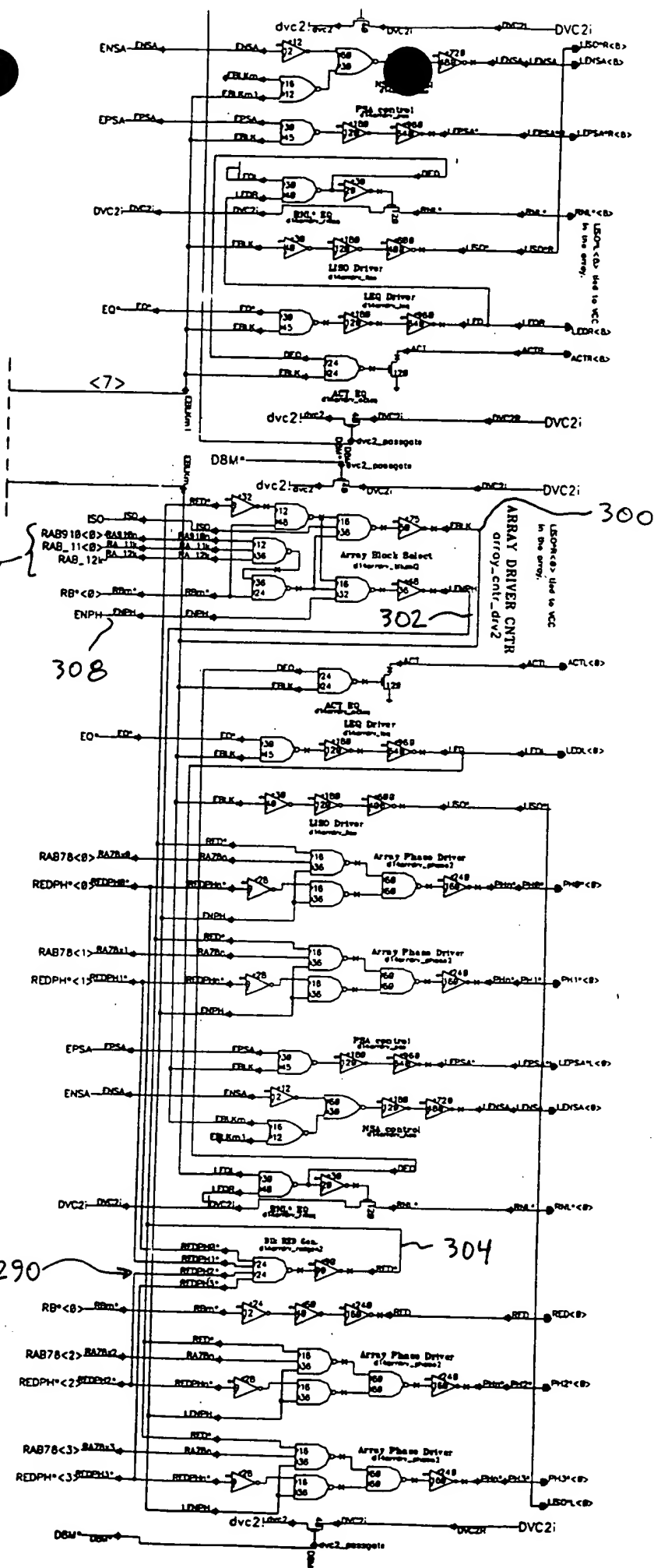


FIGURE 159

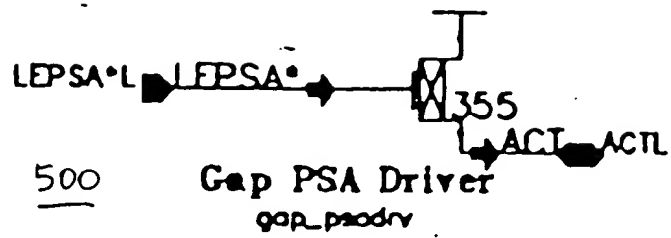


FIGURE 160

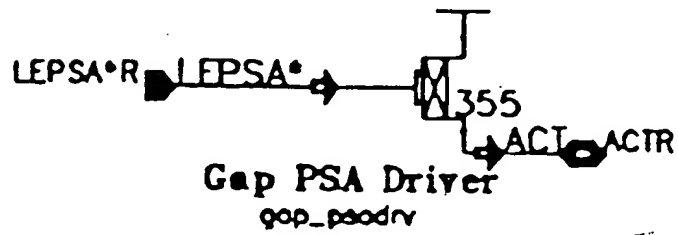


FIGURE 161



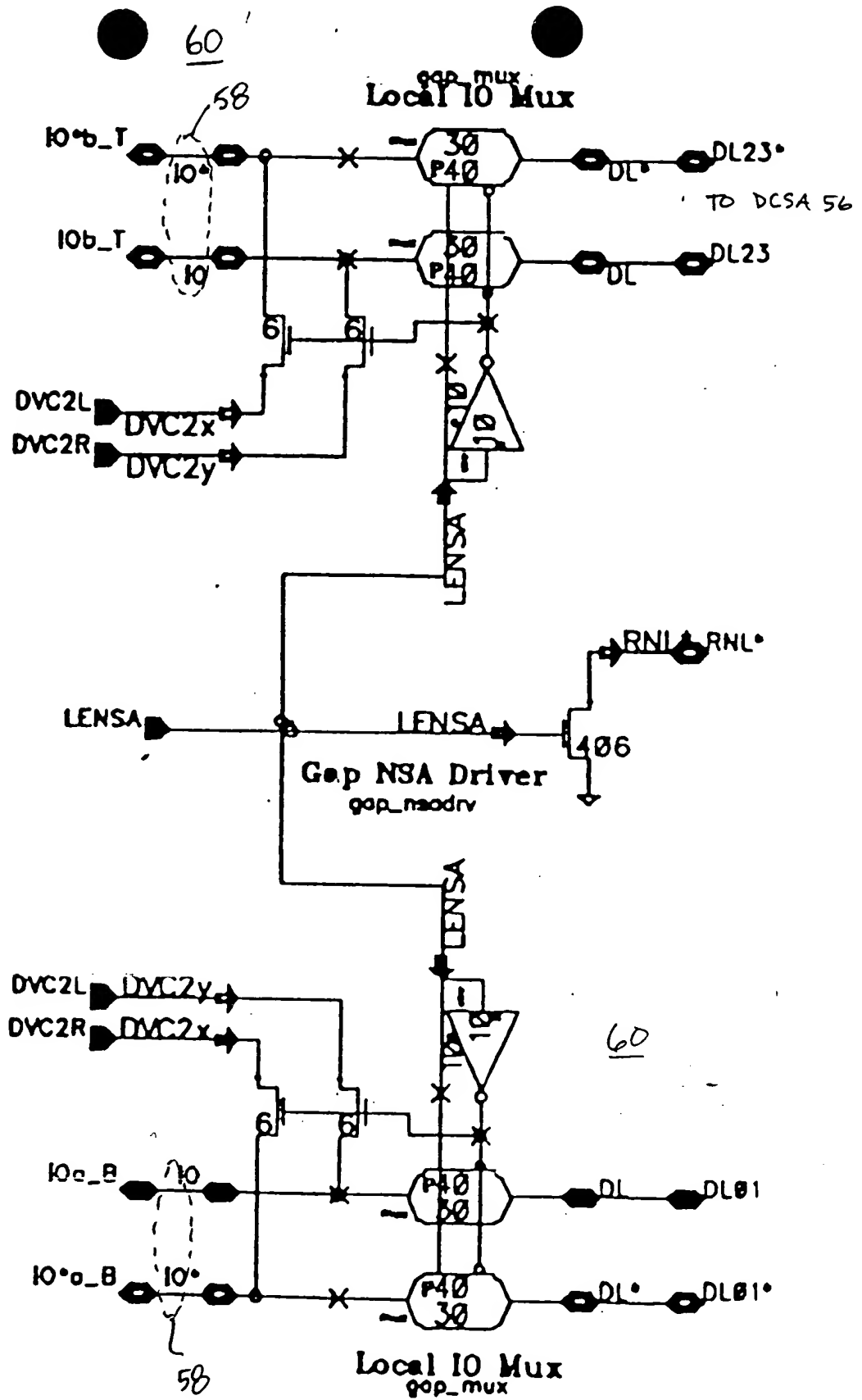


FIGURE 162

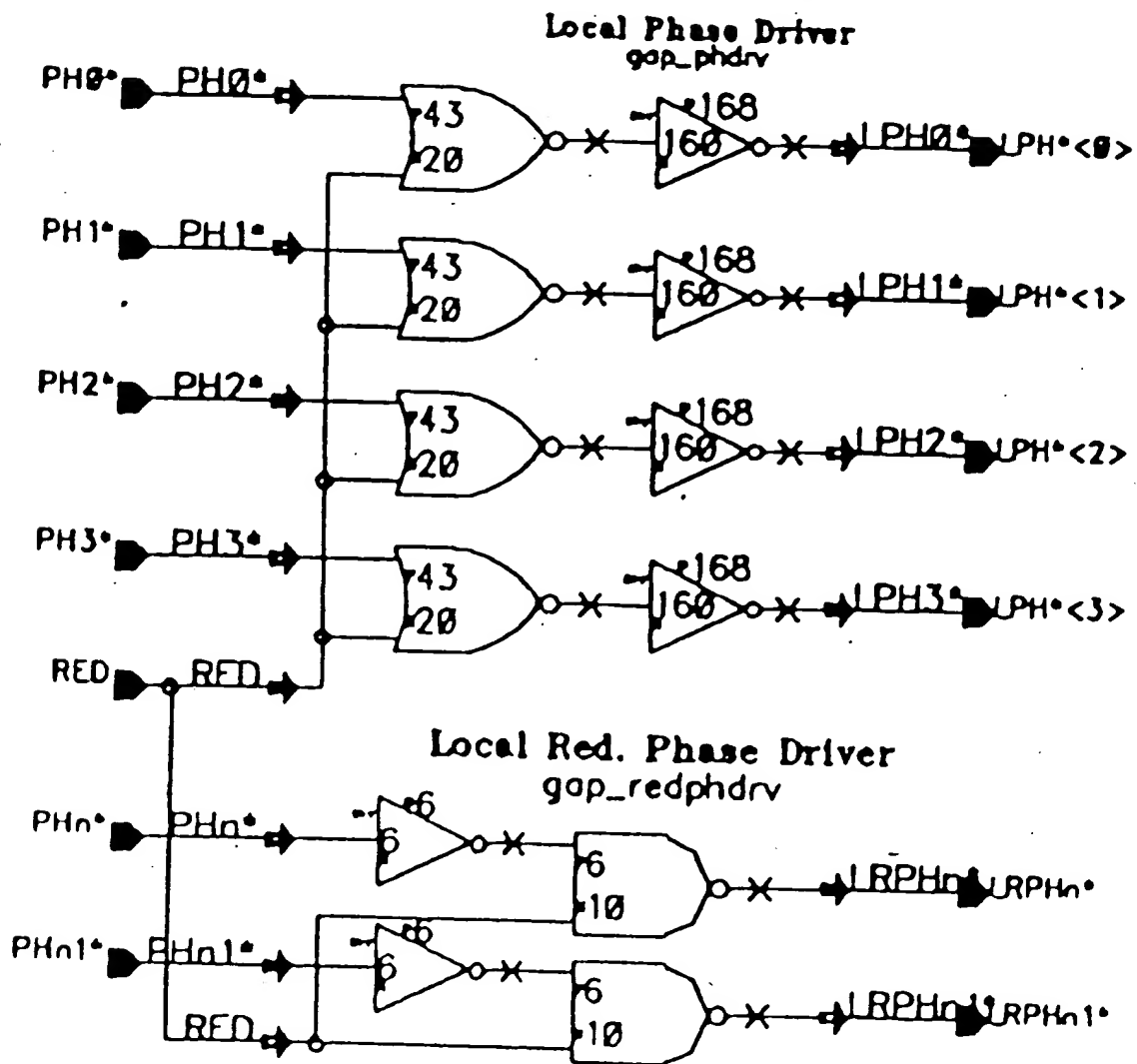
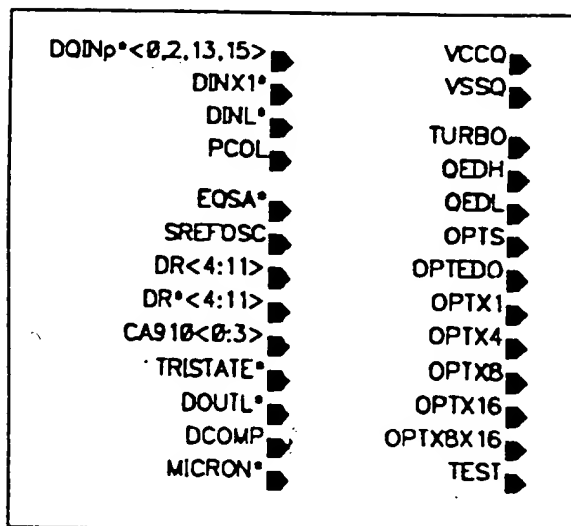


FIGURE 163

# INPUTS



# OUTPUTS

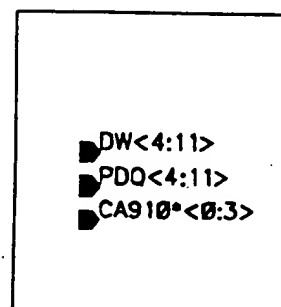


FIGURE 164

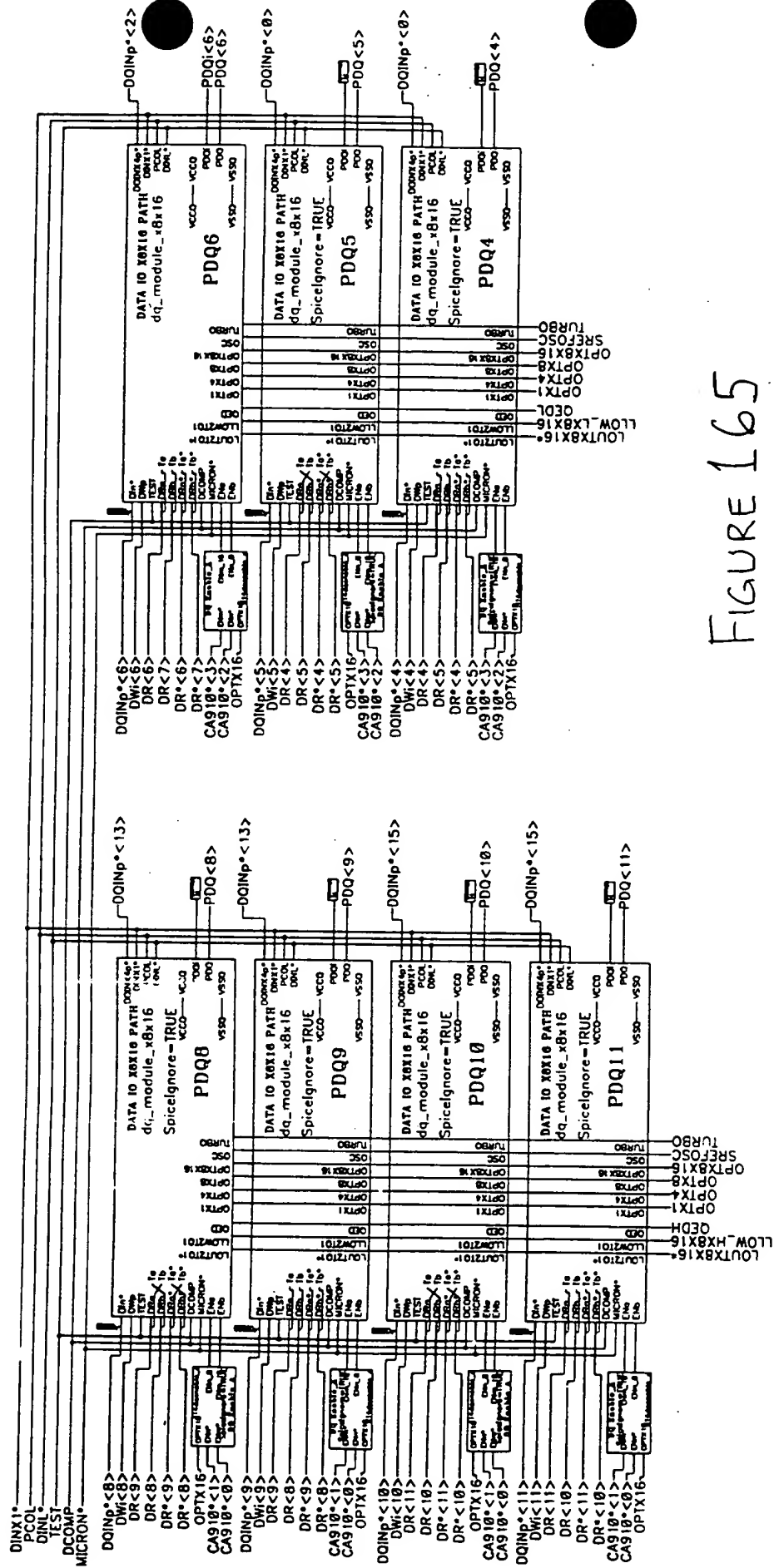


FIGURE 165

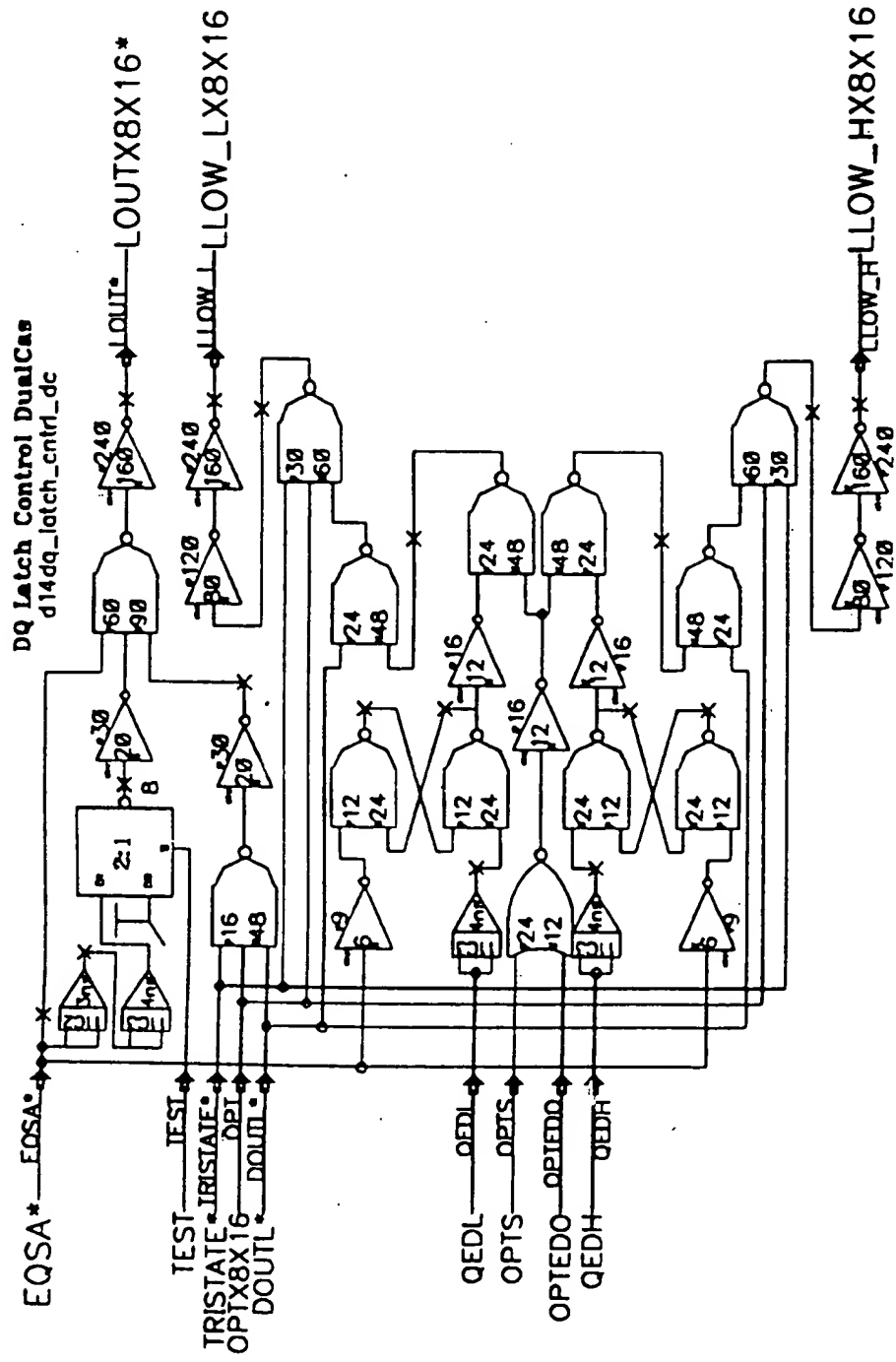


FIGURE 166

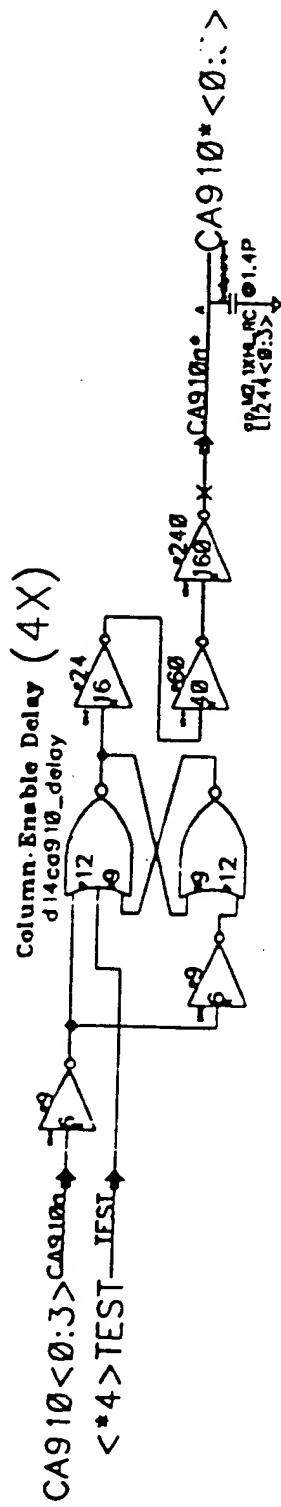


FIGURE 167

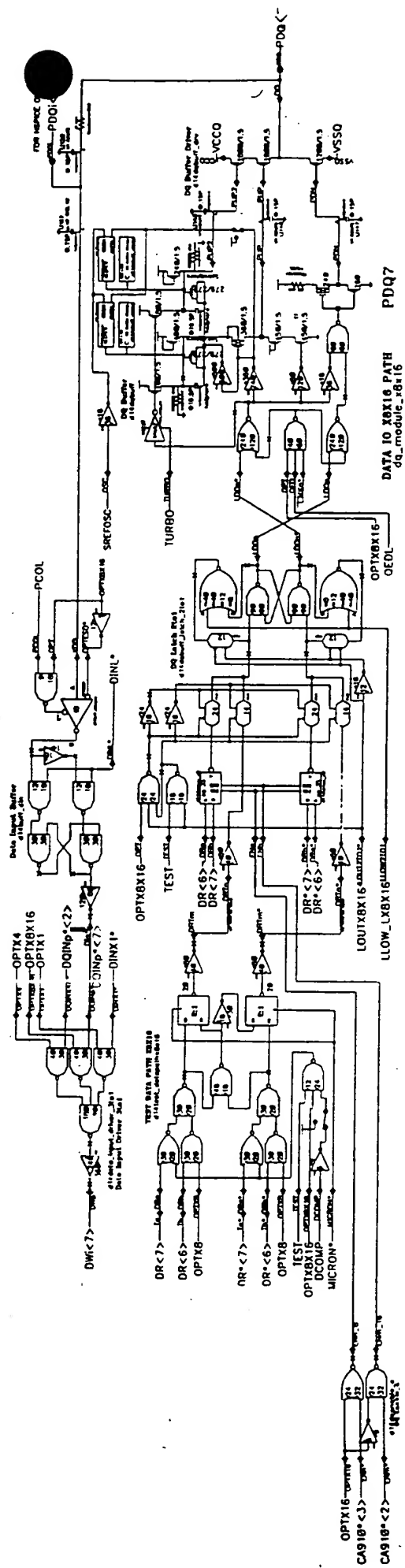


FIGURE 168

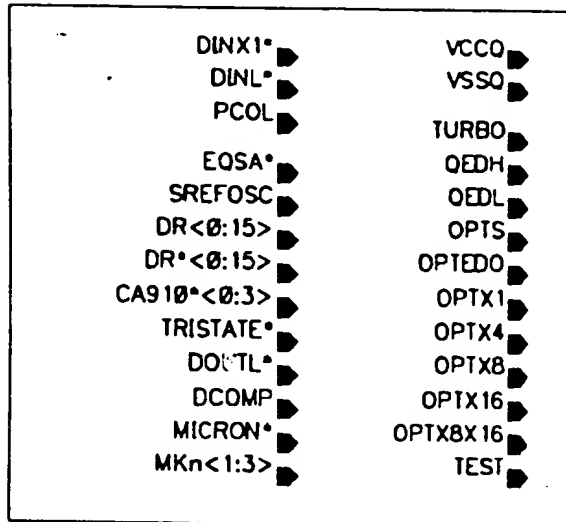
X8/X16 DQ Pads  
(DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11)

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	DW	DR/DR*
$\bar{D}Q1$	DQ0	0 1	0 1	0, 1 0, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	8 9	8 9	8, 9 8, 9
DQ6	DQ5	10 11	10 11	10, 11 10, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DQ8	DQ7	14 15	14 15	14, 15 14, 15

FIGURE 169



# INPUTS



# OUTPUTS

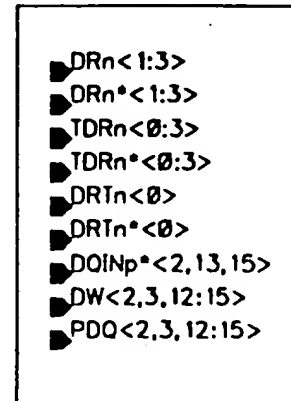


FIGURE 170

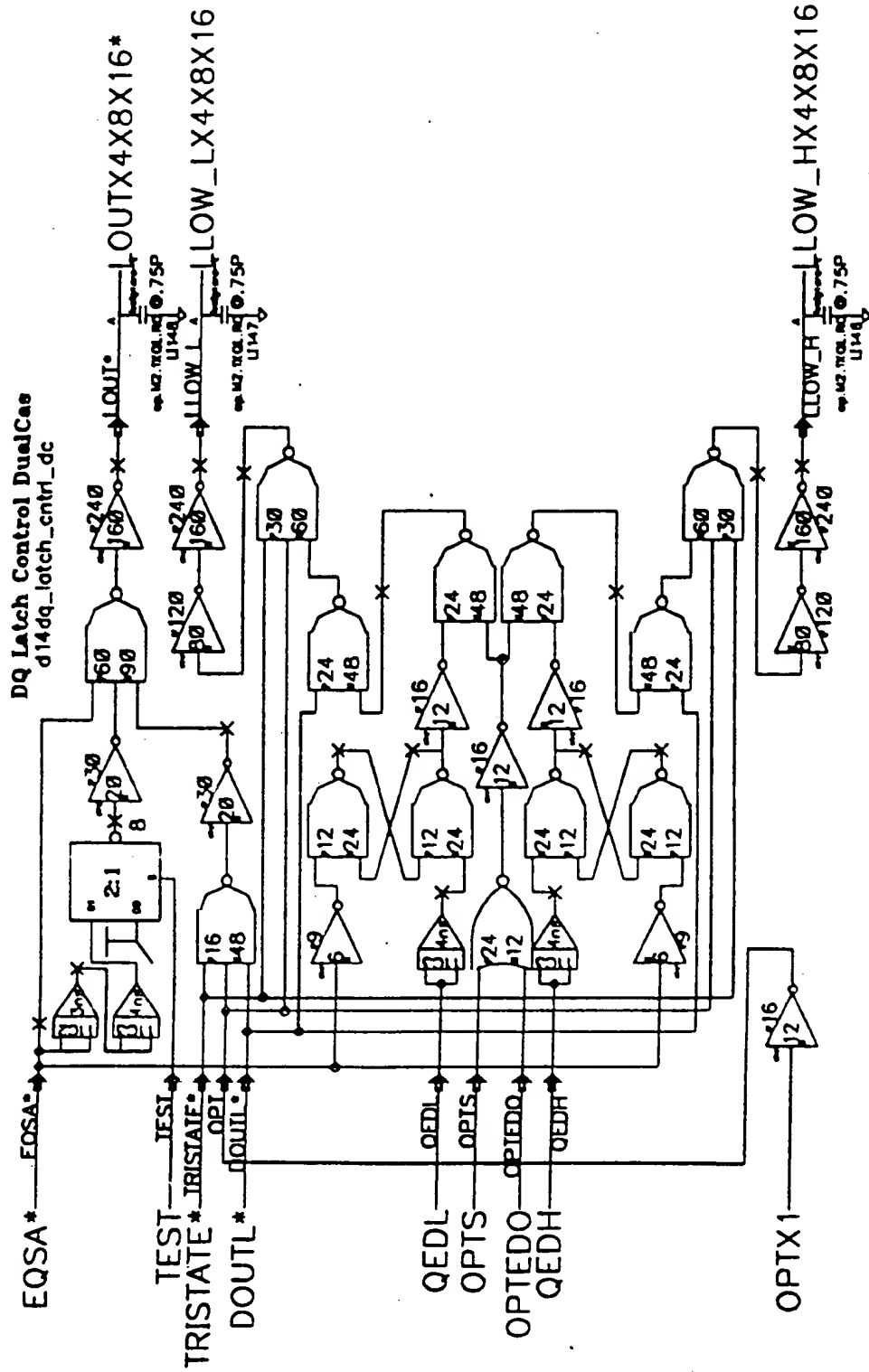


FIGURE 171

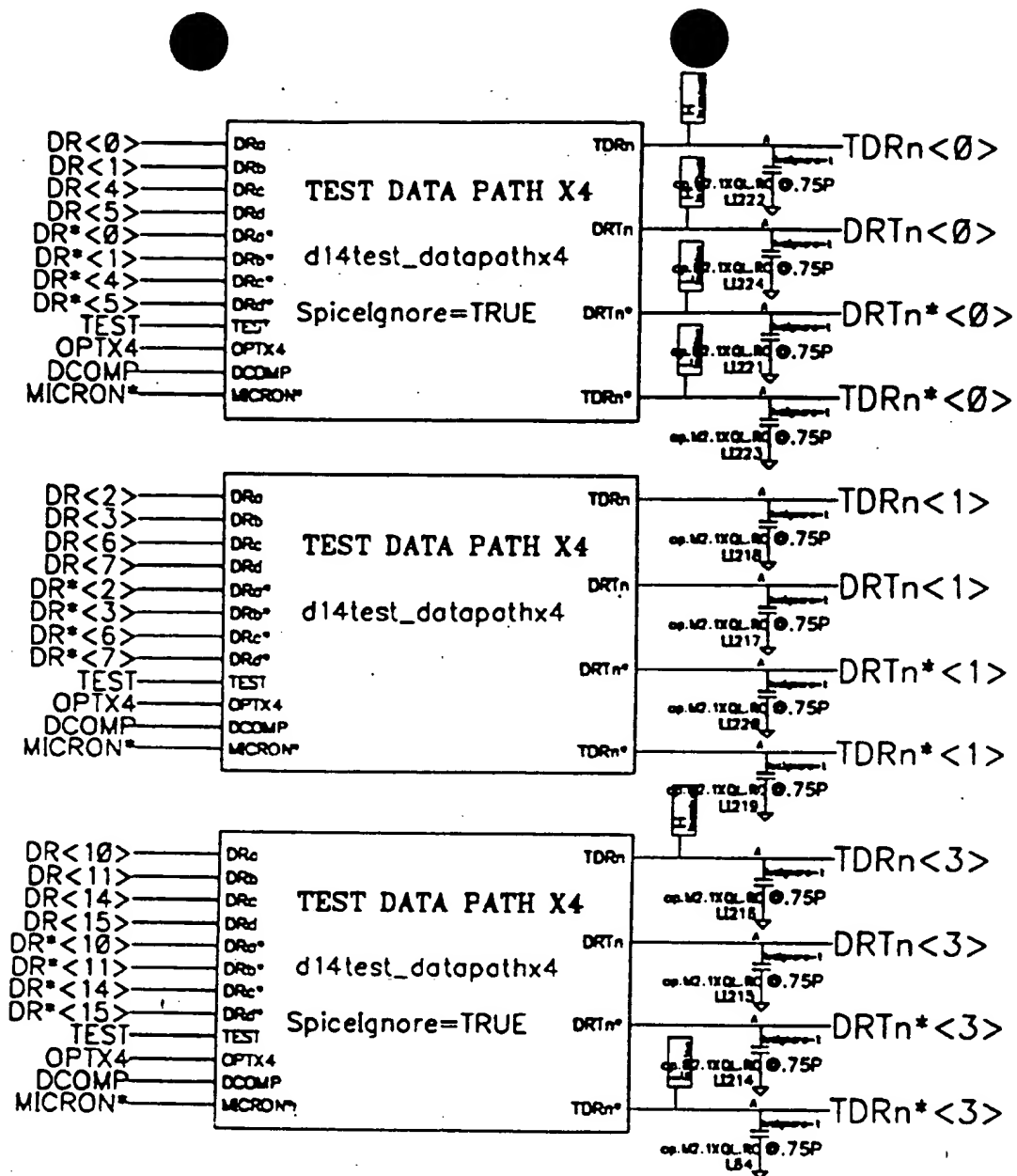


FIGURE 172

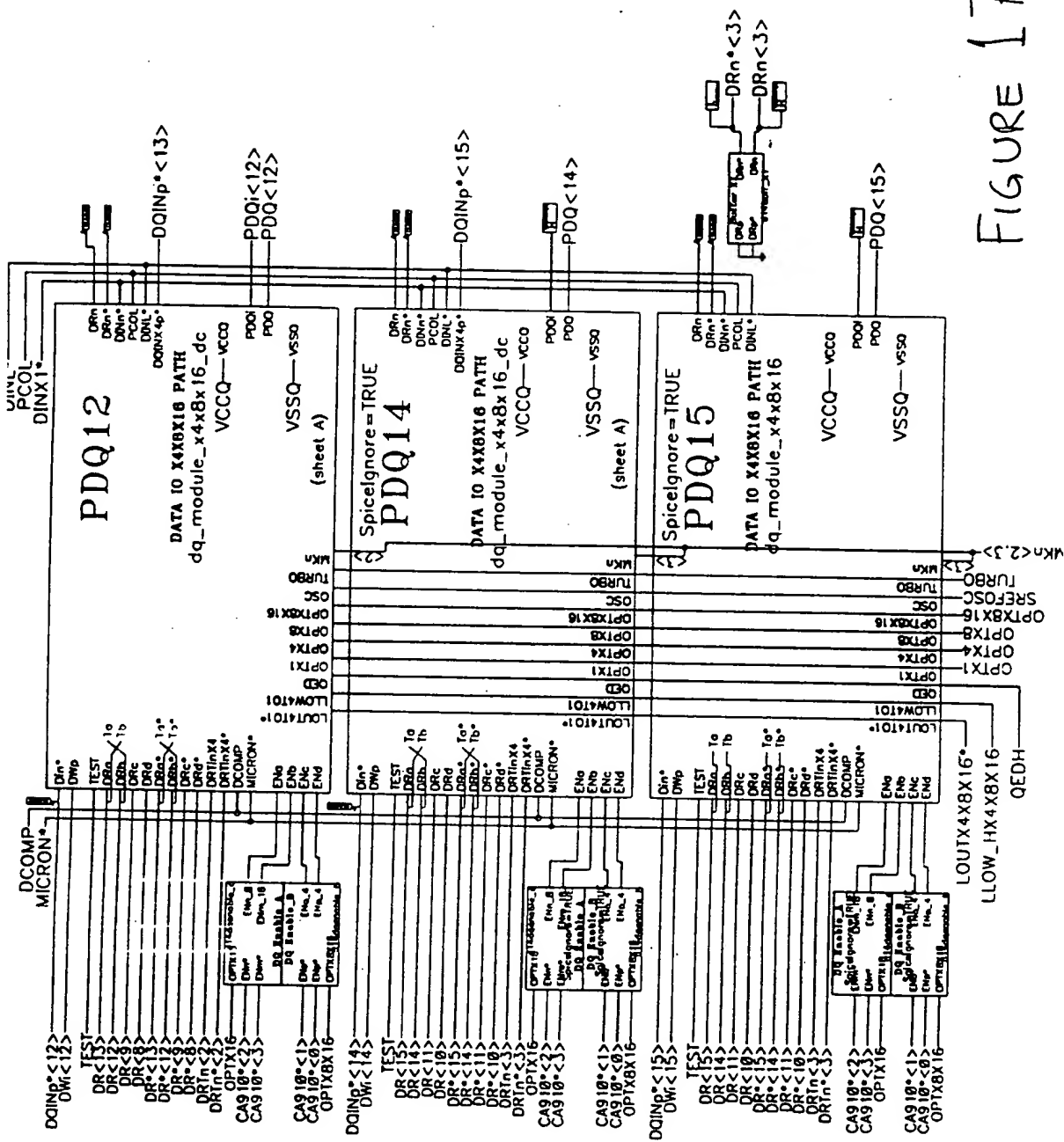


FIGURE 173

# DATA IO X4X8X16 PATH dq\_module\_x4x8x16

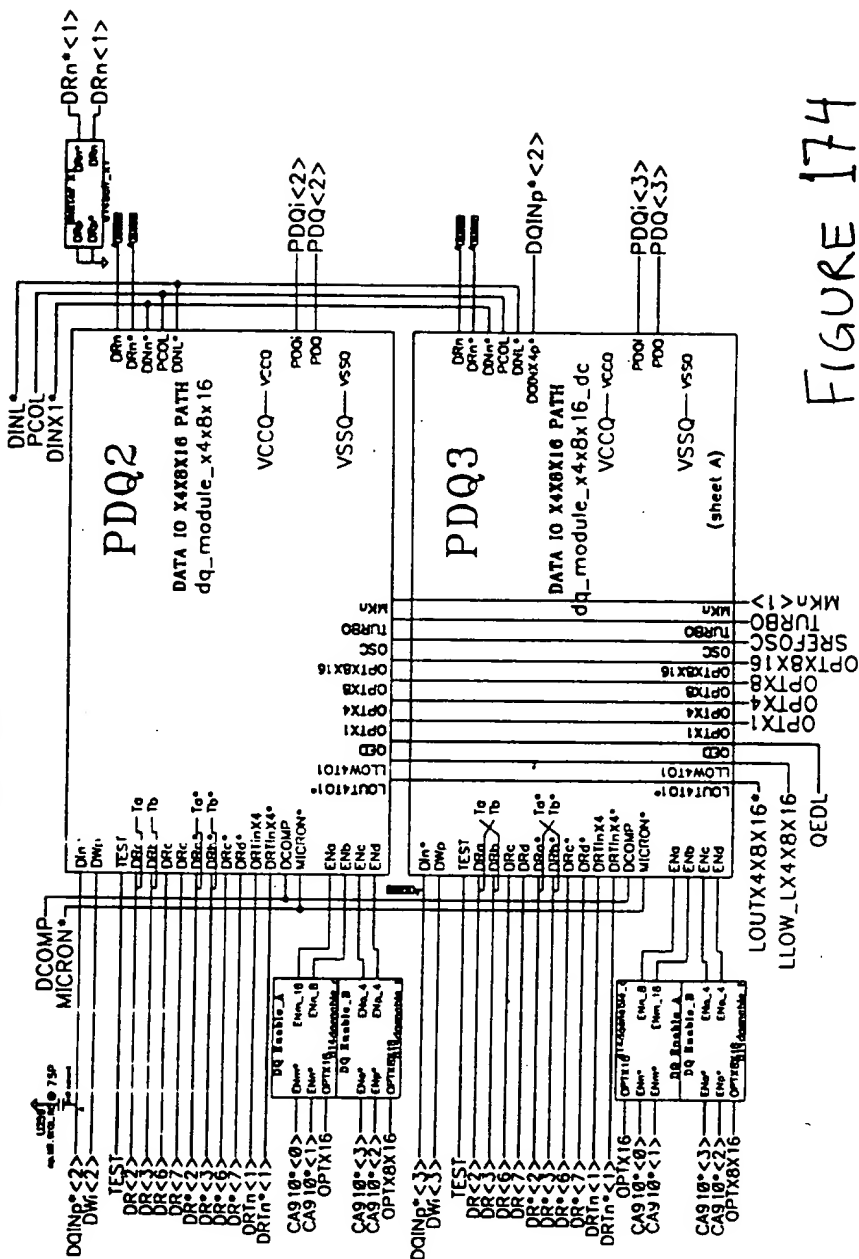


FIGURE 174



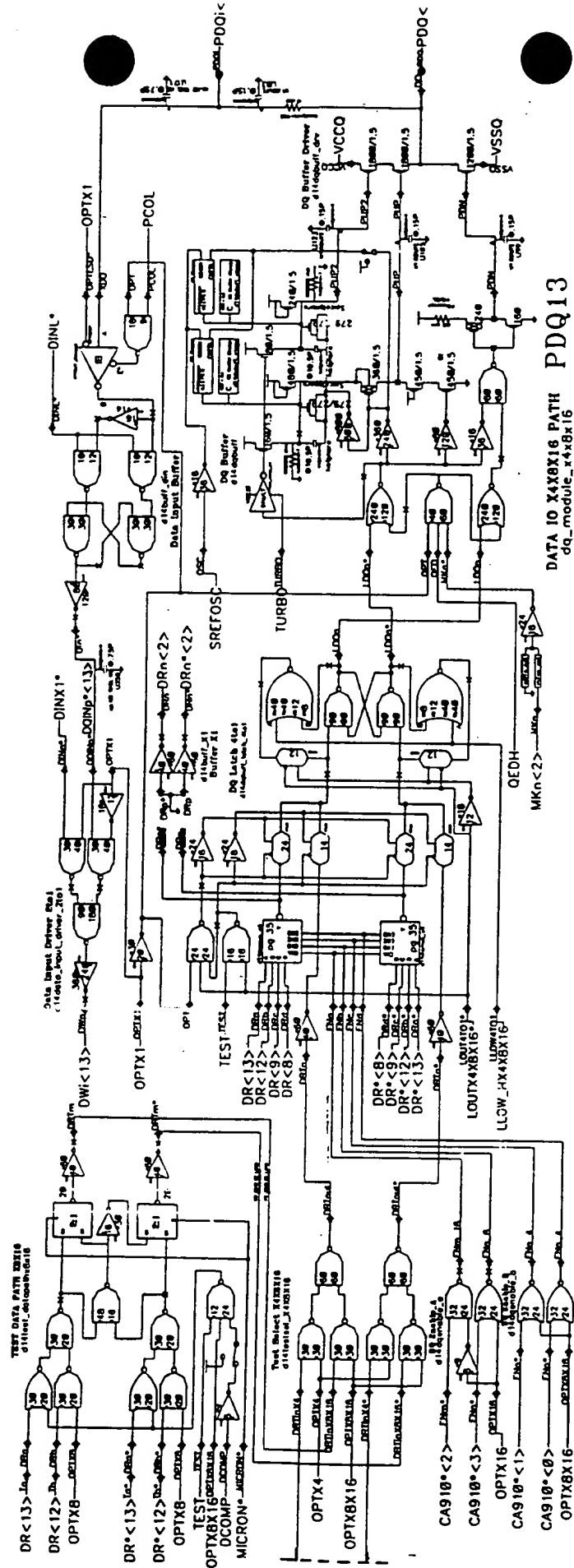
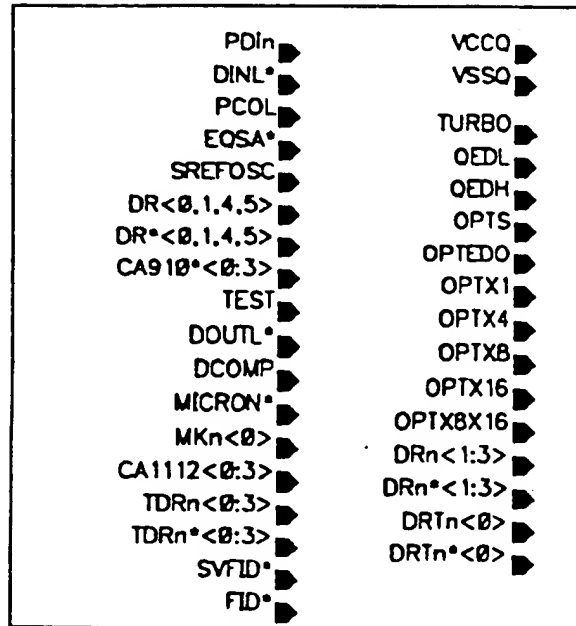


FIGURE 176

DATA IO X4X8X16 PATH  
dq\_module\_x4x8x16 PDQ13

# INPUTS



# OUTPUTS

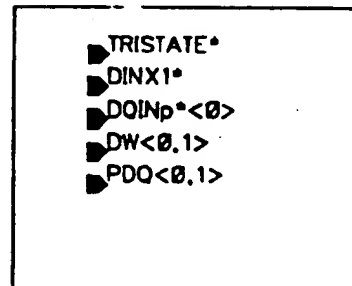


FIGURE 177



X4 Configuration

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	Data Write DW	Data Read DR/DR*
DQ1	DQ0	0	0, 4, 5	0, 1, 4, 5
		1	1	0, 1, 4, 5
DQ2	DQ1	2	2, 6, 7	2, 3, 6, 7
		3	3	2, 3, 6, 7
DQ3	DQ2	12	12	8, 9, 12, 13
		13	13, 8, 9	8, 9, 12, 13
DQ4	DQ3	14	14	10, 11, 14, 15
		15	15, 10, 11	10, 11, 14, 15

X1 Configuration (see next page)

DR/DR*	Bond Pad Assembly PDQ	Pin-out
DRn<0>	PDQ0 (DOUT)	
DRn<1>		
DRn<2>		
DRn<3>		

FIGURE 178

DQ Compression

DR/DW	PDQ	X8 DQ	X16 DQ
0,1,4,5	0,1	0	0
2,3,6,7	2,3	1	2
8,9,12,13	12,13	6	13
10,11,14,15	14,15	7	15

FIGURE 179

DATA IN (X1)

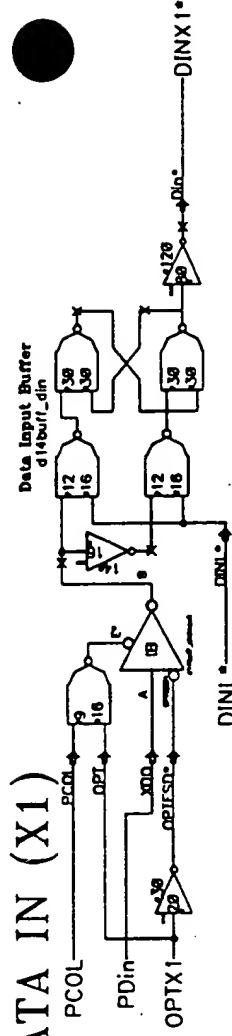


FIGURE 180

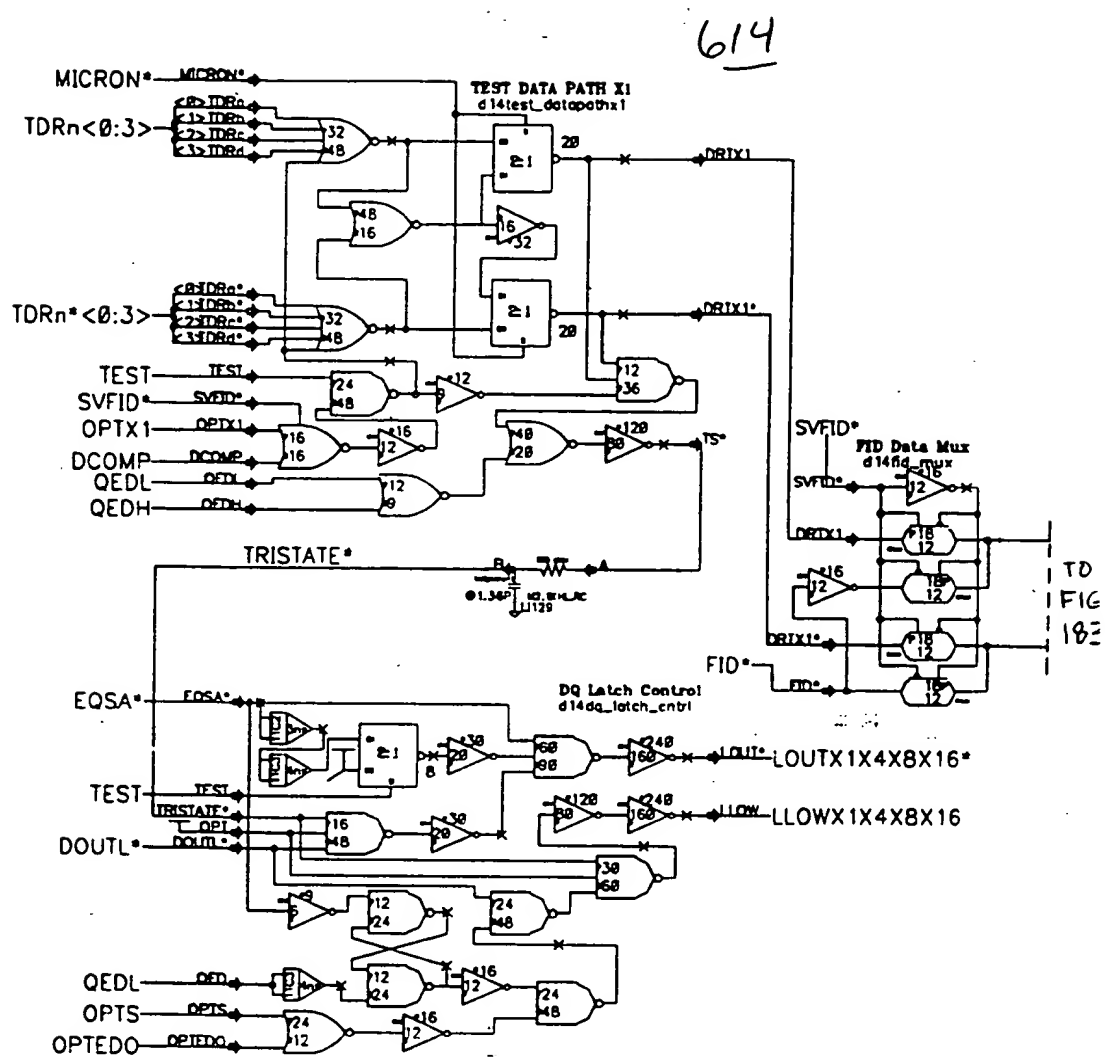


FIGURE 182

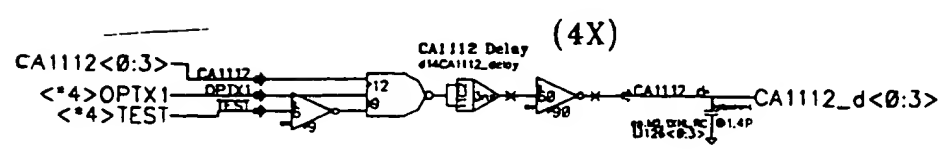
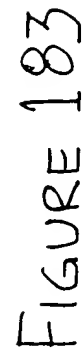


FIGURE 181



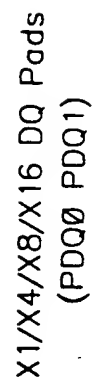


FIGURE 184

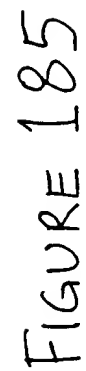
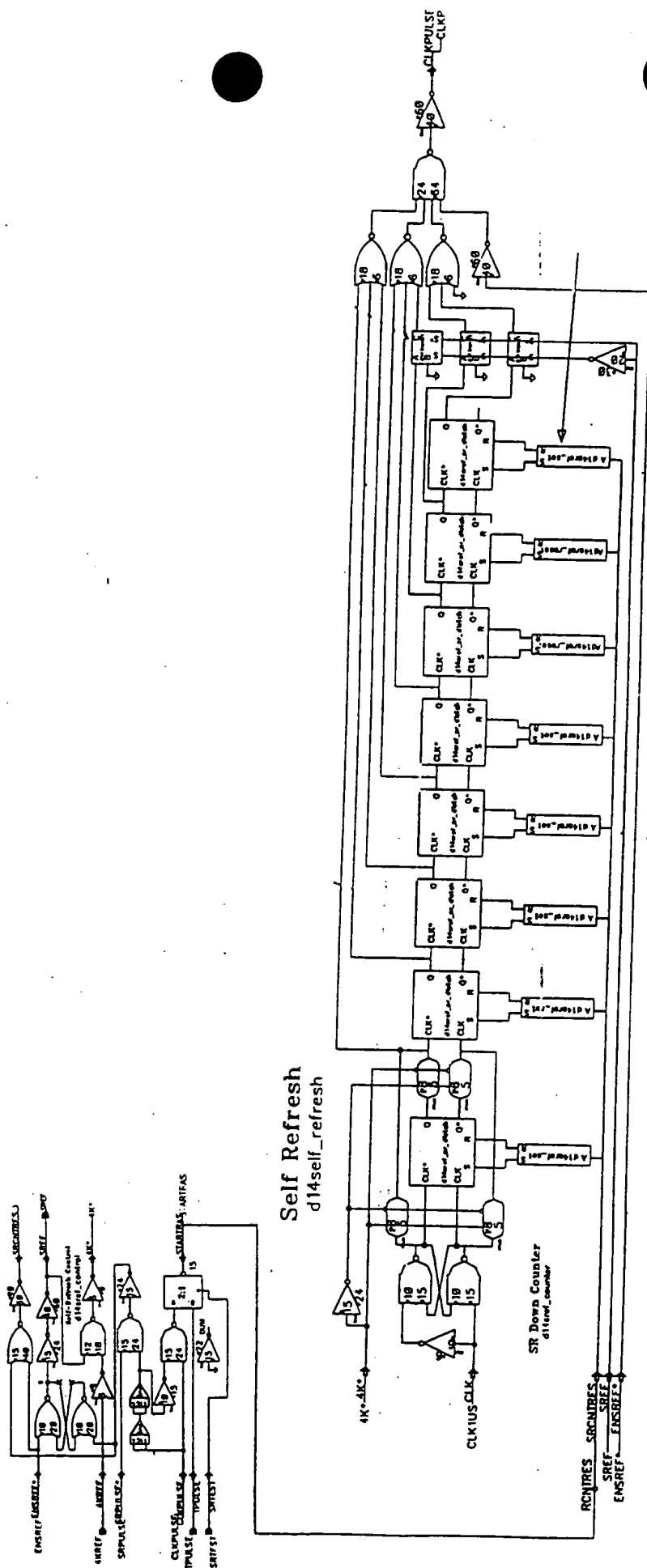


FIGURE 185





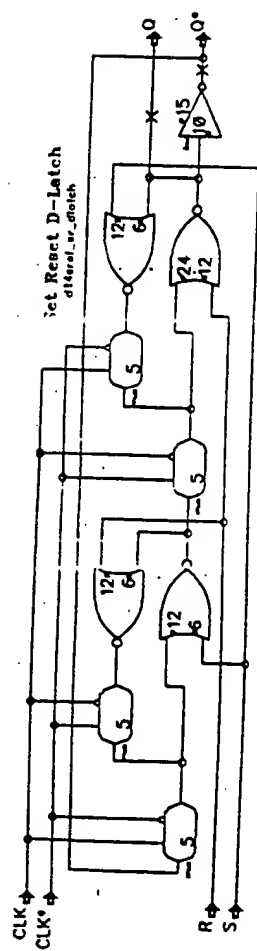


FIGURE 188

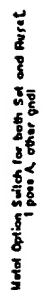


FIGURE 189

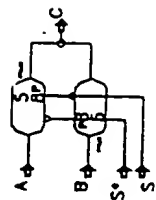


FIGURE 191

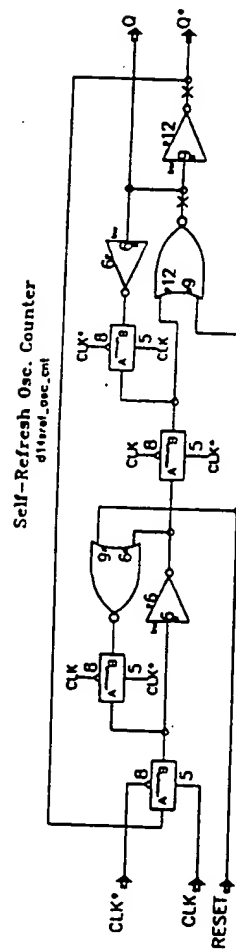


FIGURE 19D



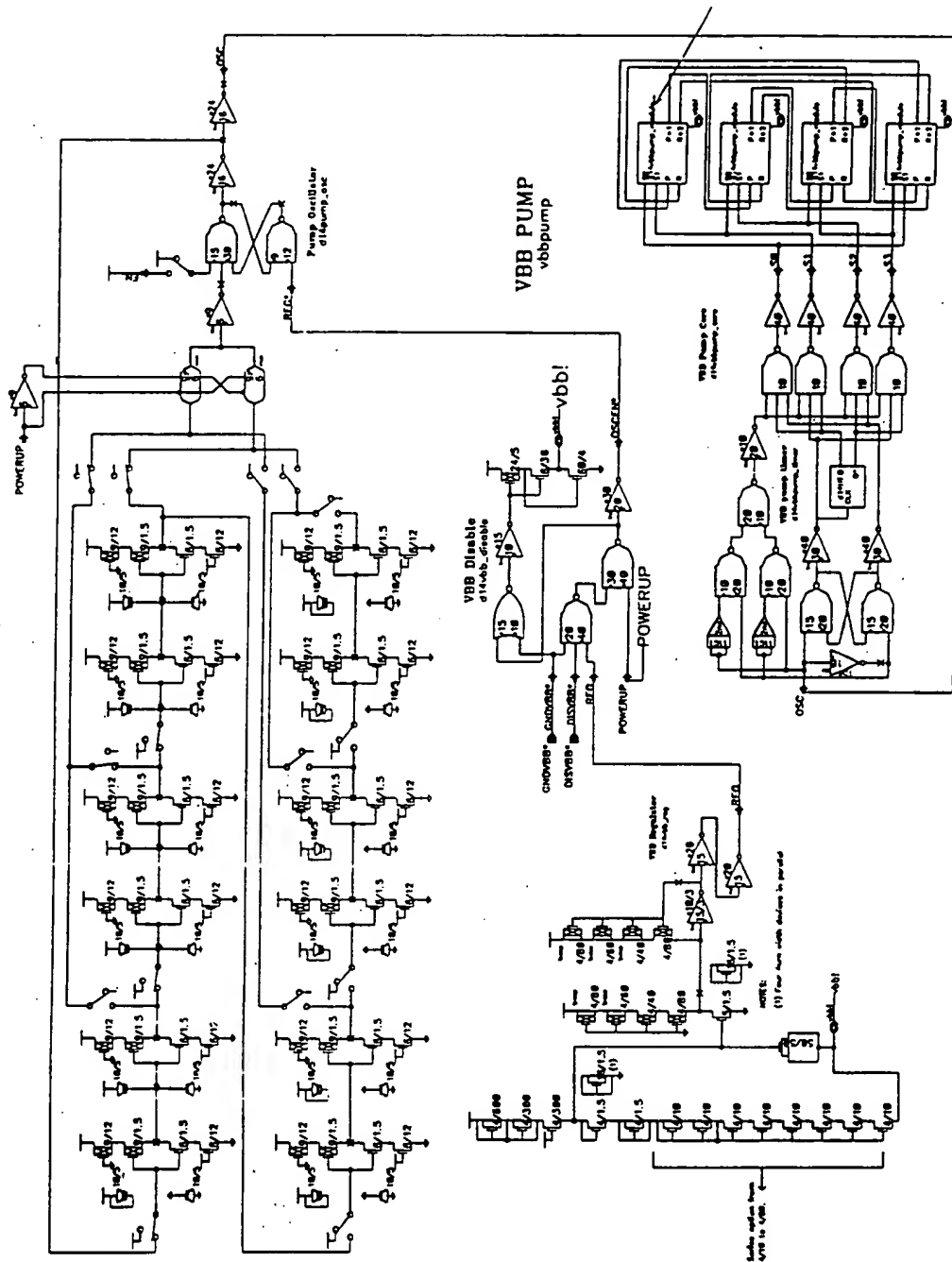


FIGURE 192

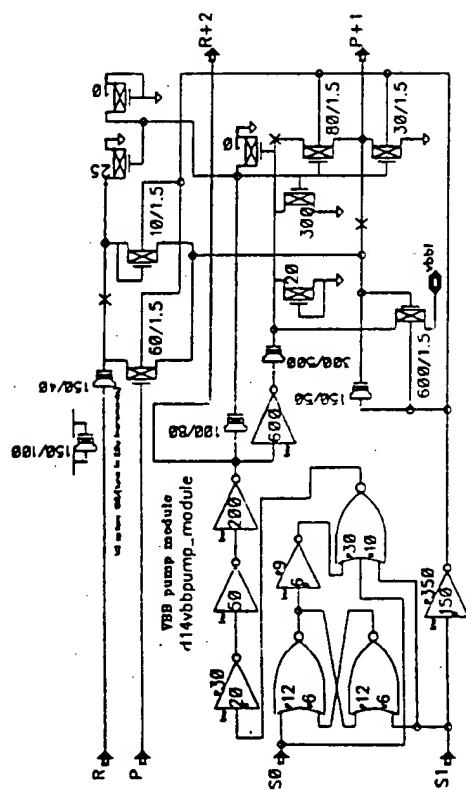


FIGURE 193

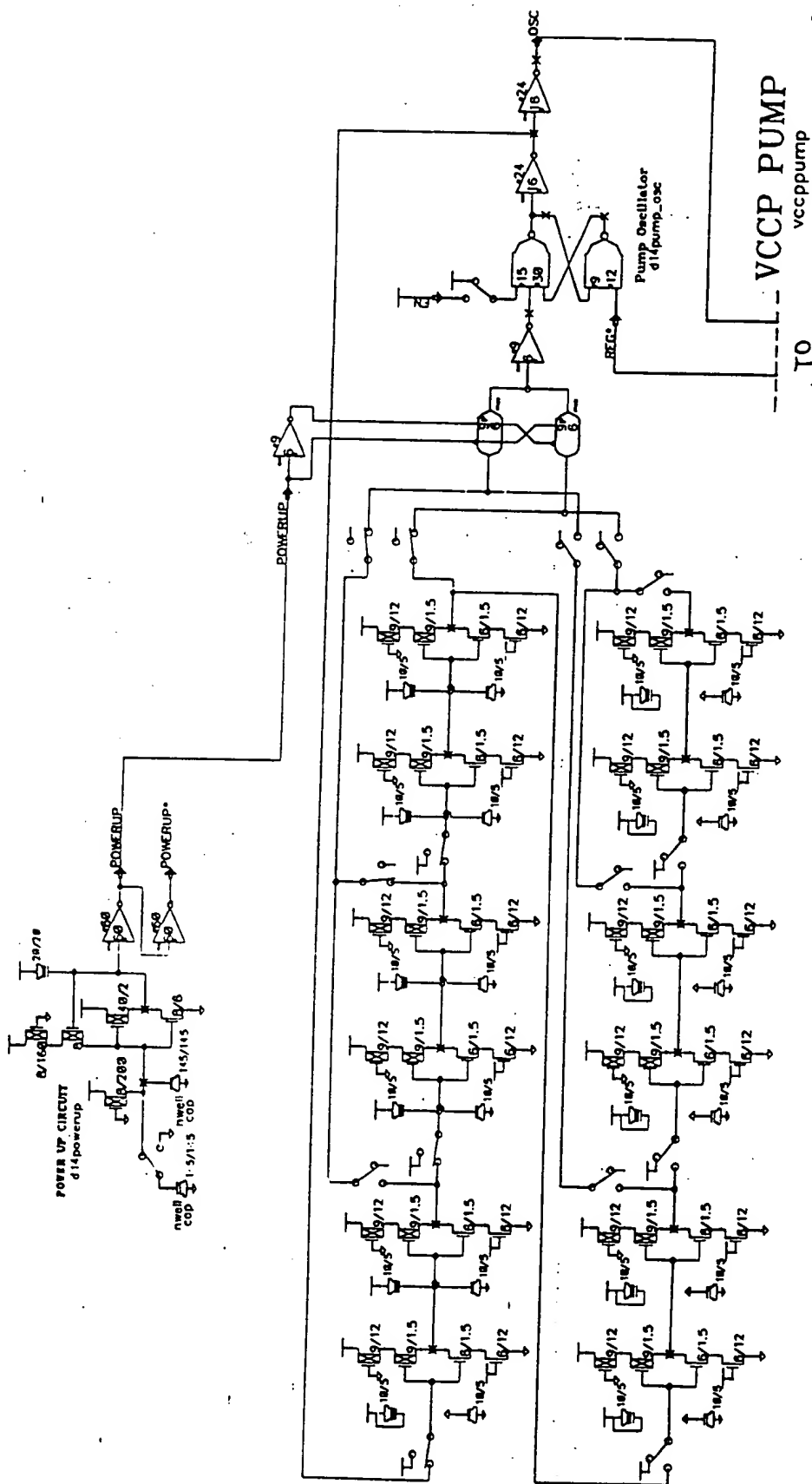


FIGURE 194

FIGURE  
195

FROM FIGURE 194

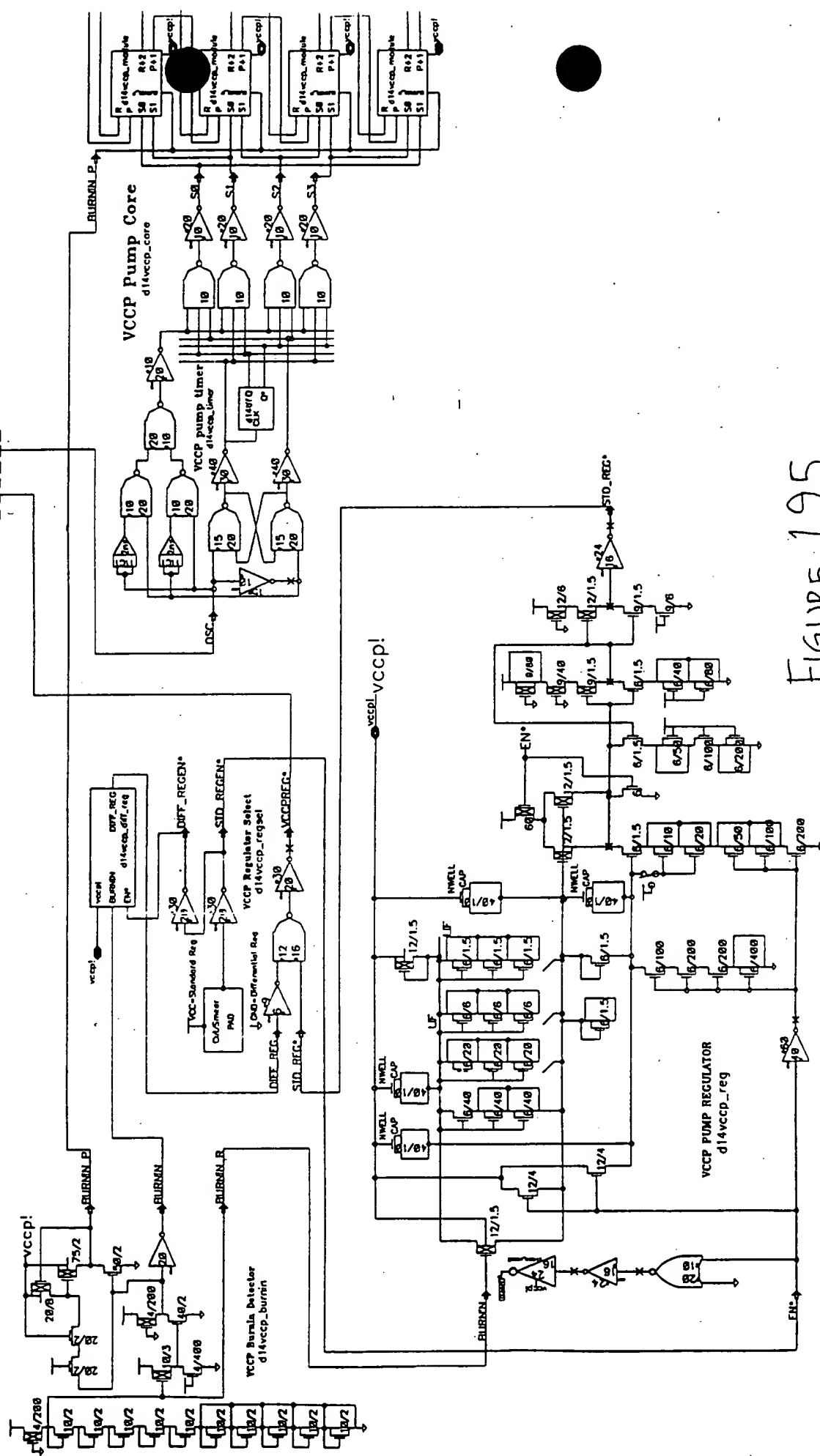
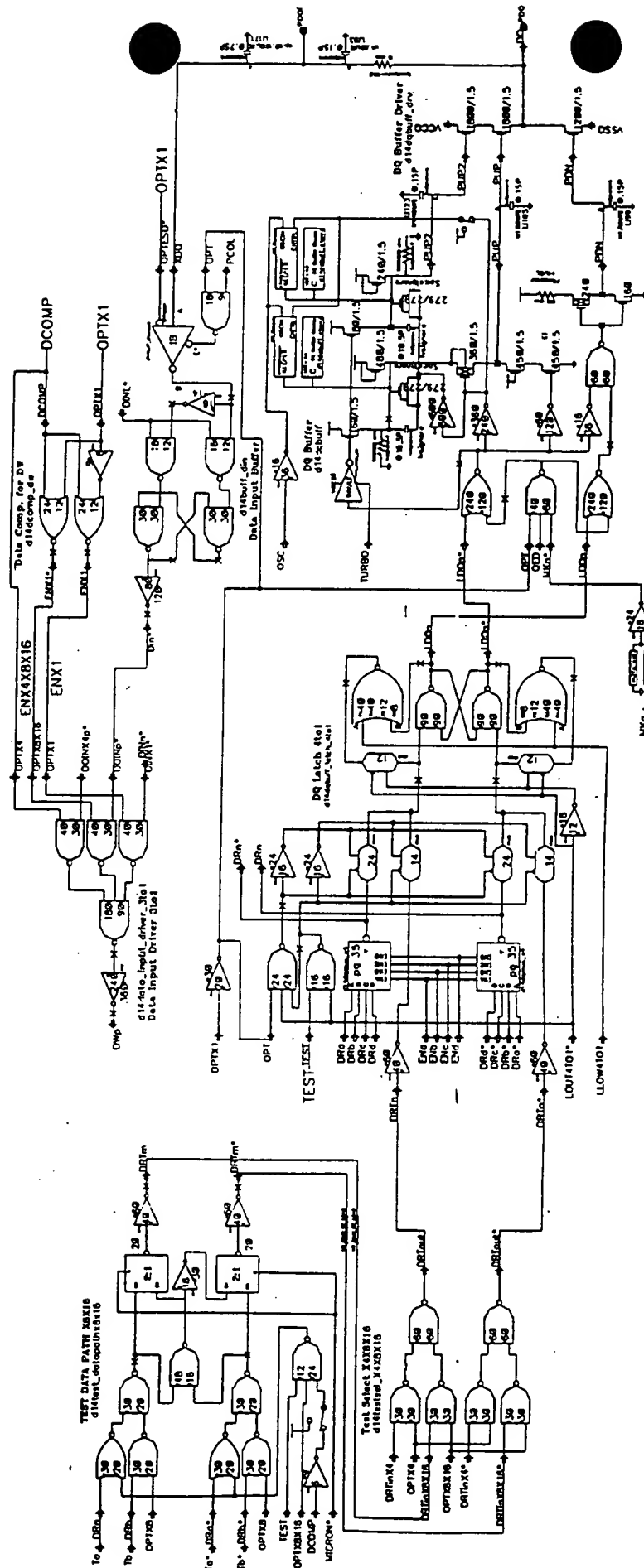


FIGURE 195









DATA IO X4XB16 PATH  
dq\_module\_x4xb16\_dc

FIGURE 200



DQ Buffer Clamp  
d14dqbuff\_clamp

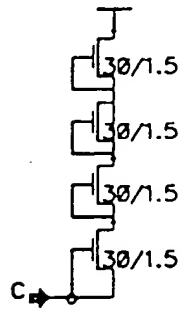


FIGURE 201

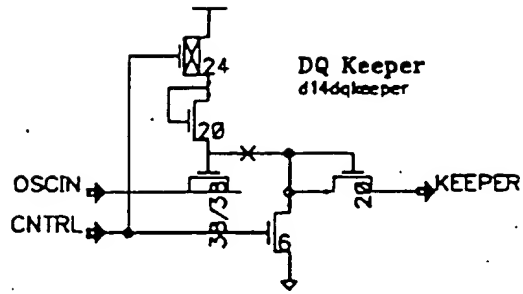


FIGURE 202

1020

1030

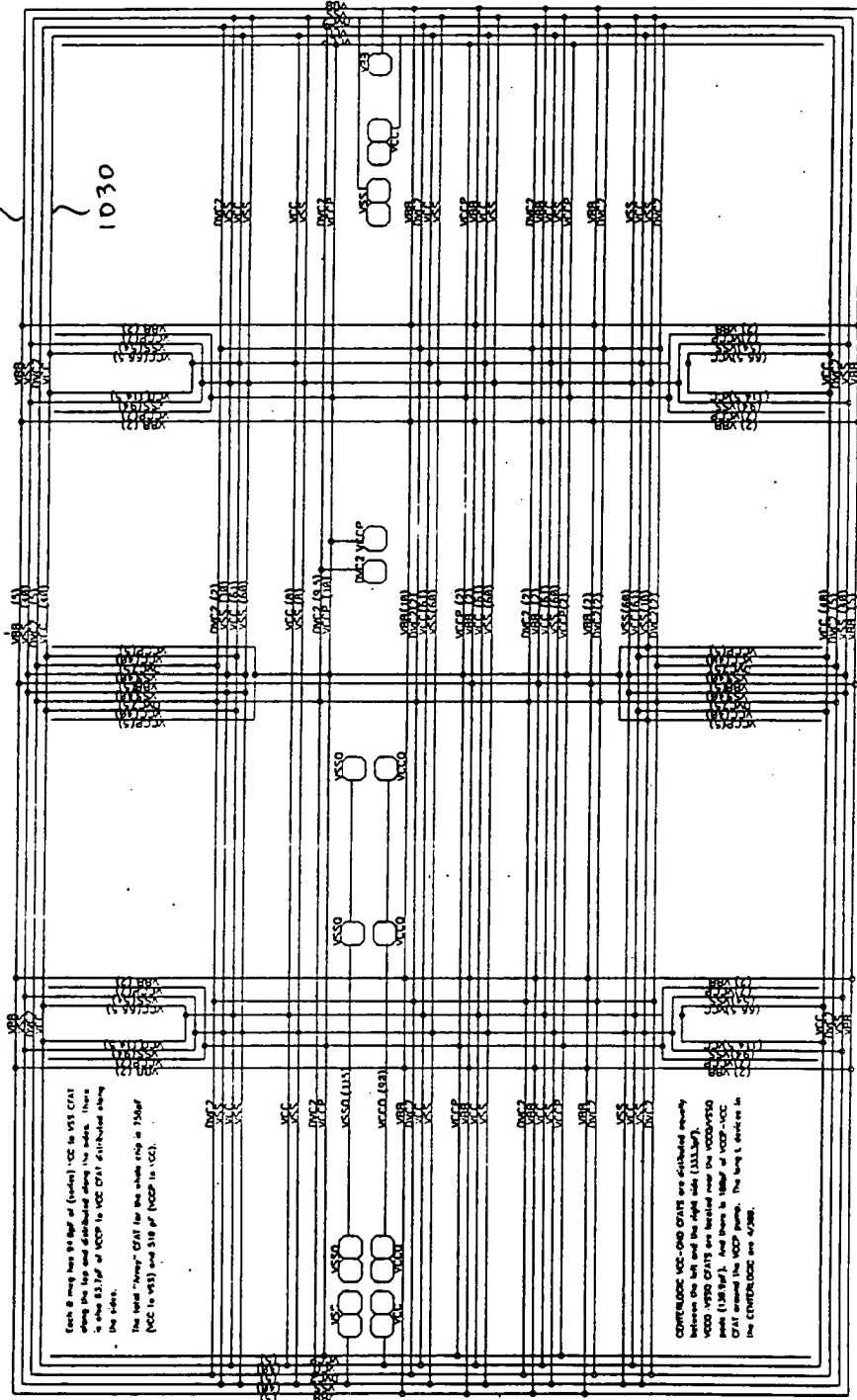


FIGURE 203

CONFIG	ROW ADDRESS		COLUMN ADDRESS	
	8K refresh	4K refresh	8K refresh	4K refresh
4MX16	A0 – A12	A0 – A11	A0 – A8	A0 – A9
8MX8	A0 – A12	A0 – A11	A0 – A9	A0 – A10
16MX4	A0 – A12	–	A0 – A10	A0 – A11
64MX1	A0 – A12	–	A0 – A12	–

FIGURE 204

Test Mode Address Compression (ref to X1)	
The following column addresses are ignored	
16X	A12, A11, A10, A9
32X	A12, A11, A10, A9, A8 (default customer testmode)
64X	A12, A11, A10, A9, A8, A7
128X	A12, A11, A10, A9, A8, A7, plus row address A12

FIGURE 205

## DQ Configuration

(X16)	(X8)	(X4)	(X16)	(X8)	(X4)	(X1)
DQ5	DQ2	DQ0	DQ4	DQ2	DQ0	CA1112<0>
DQ7	DQ3	DQ1	DQ6	DQ3	DQ1	CA1112<1>
DQ13	DQ6	DQ2	DQ12	DQ6	DQ2	CA1112<2>
DQ15	DQ7	DQ3	DQ14	DQ7	DQ3	CA1112<3>
CA910<2>			CA910<3>			
DQ10	DQ5	DQ3	DQ11	DQ5	DQ3	CA1112<3>
DQ8	DQ4	DQ2	DQ9	DQ4	DQ2	CA1112<2>
DQ2	DQ1	DQ1	DQ3	DQ1	DQ1	CA1112<1>
DQ0	DQ0	DQ0	DQ1	DQ0	DQ0	CA1112<0>
CA910<0>			CA910<1>			

FIGURE 206

## X8 Configuration

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	DW	DR/DR*
DQ1	DQ0	0 1	0 1	0, 1 0, 1
DQ2	DQ1	2 3	2 3	2, 3 2, 3
DQ3	DQ2	4 5	4 5	4, 5 4, 5
DQ4	DQ3	6 7	6 7	6, 7 6, 7
DQ5	DQ4	8 9	8 9	8, 9 8, 9
DQ6	DQ5	10 11	10 11	10, 11 10, 11
DQ7	DQ6	12 13	12 13	12, 13 12, 13
DQ8	DQ7	14 15	14 15	14, 15 14, 15

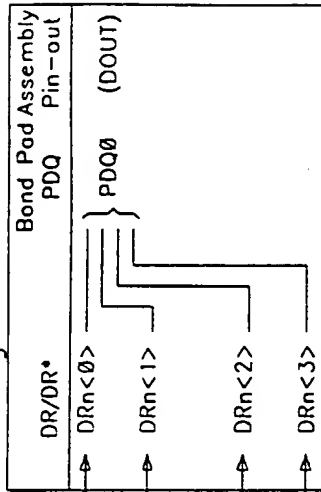
FIGURE 207

X4 Configuration

Assembly Pin-out	Schematic Pin-out	Bond Pad PDQ	Data Write DW	Data Read DR/DR*
DQ1	DQ0	0	0, 4, 5	0, 1, 4, 5
		1	1	0, 1, 4, 5
DQ2	DQ1	2	2, 6, 7	2, 3, 6, 7
		3	3	2, 3, 6, 7
DQ3	DQ2	12	12	8, 9, 12, 13
		13	13, 8, 9	8, 9, 12, 13
DQ4	DQ3	14	14	10, 11, 14, 15
		15	15, 10, 11	10, 11, 14, 15

FIGURE 208

X1 Configuration



DQ Compression

DR/DW	X8 Config PDQ Assembly DQ	X16 Config PDQ Assembly DQ
0,1,4,5	0,1	1
2,3,6,7	2,3	2
8,9,12,13	12,13	7
10,11,14,15	14,15	8
		15
		16

FIGURE 209

Address Compression

CONFIG	ROW ADDRESS 8K ref	ROW ADDRESS 4K ref	COLUMN ADDRESS 8K ref	COLUMN ADDRESS 4K ref
4MX16	A0 - A12	A0 - A11	A0 - A8	A0 - A9
8MX8	A0 - A12	A0 - A11	A0 - A9	A0 - A10
16MX4	A0 - A12	A0 - A11	A0 - A10	A0 - A11
64MX1	A0 - A12	-	A0 - A12	-

FIGURE 210

Test Mode Address Compression (ref to X1)  
The following column addresses are ignored

16X	A12, A11, A10, A9
32X	A12, A11, A10, A9, A8
64X	A12, A11, A10, A9, A8, A7
128X	A12, A11, A10, A9, A8, A7, RA12

FIGURE 211

## Cancel Row Fusebank

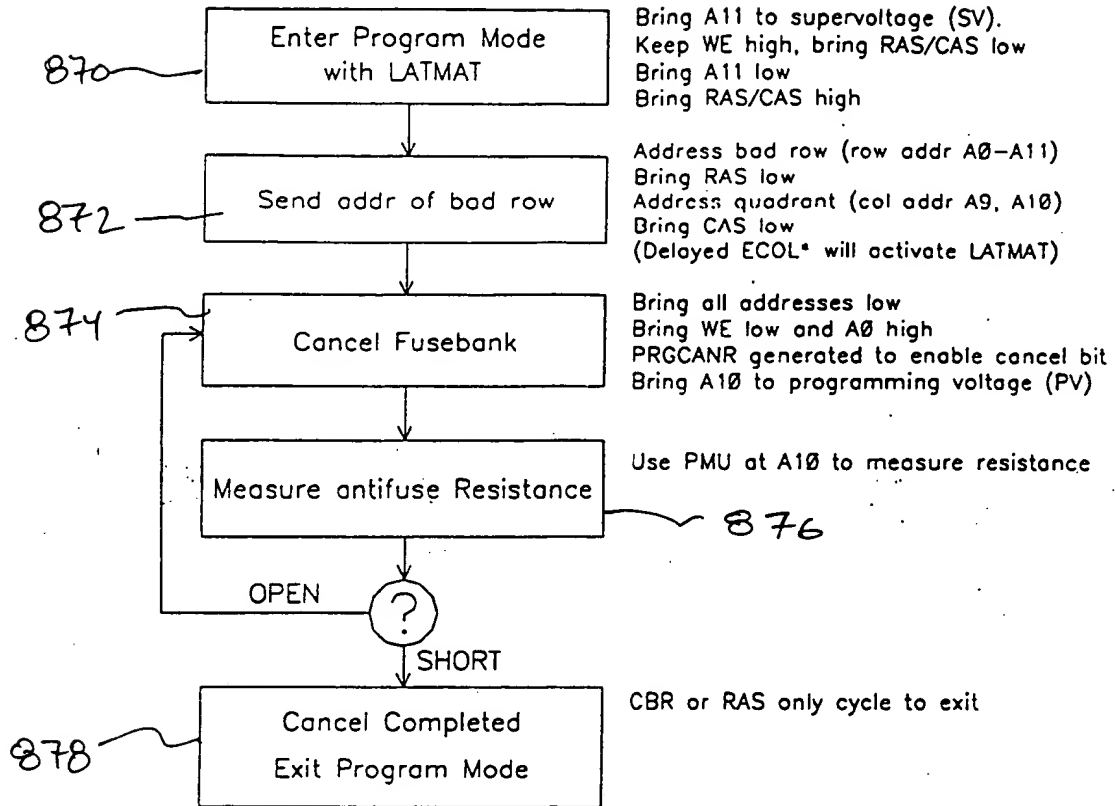


FIGURE 213

# Locate Usable Electrical Fusebank and Determine Need for Cancel

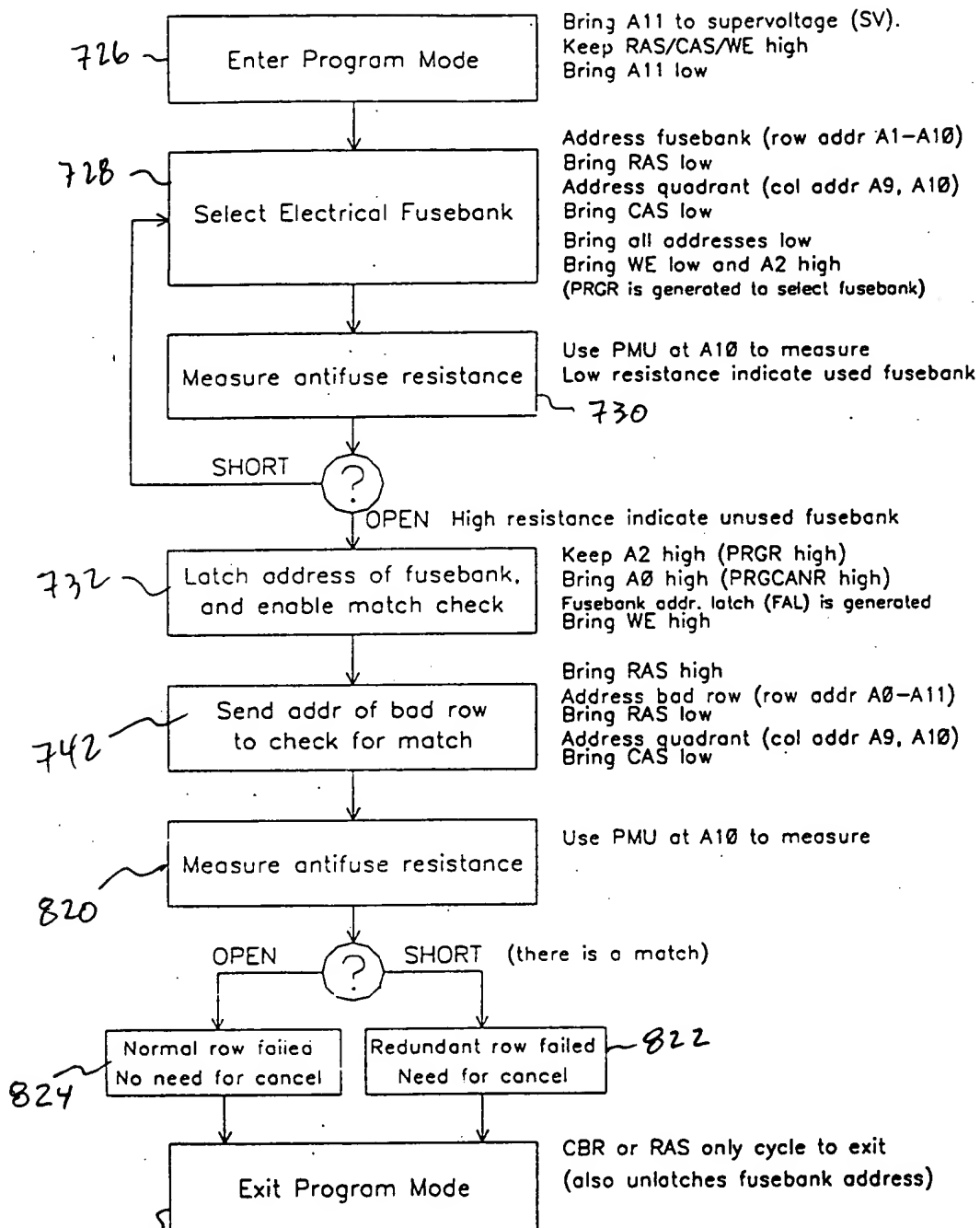


FIGURE 212

## Cancel Row Fusebank

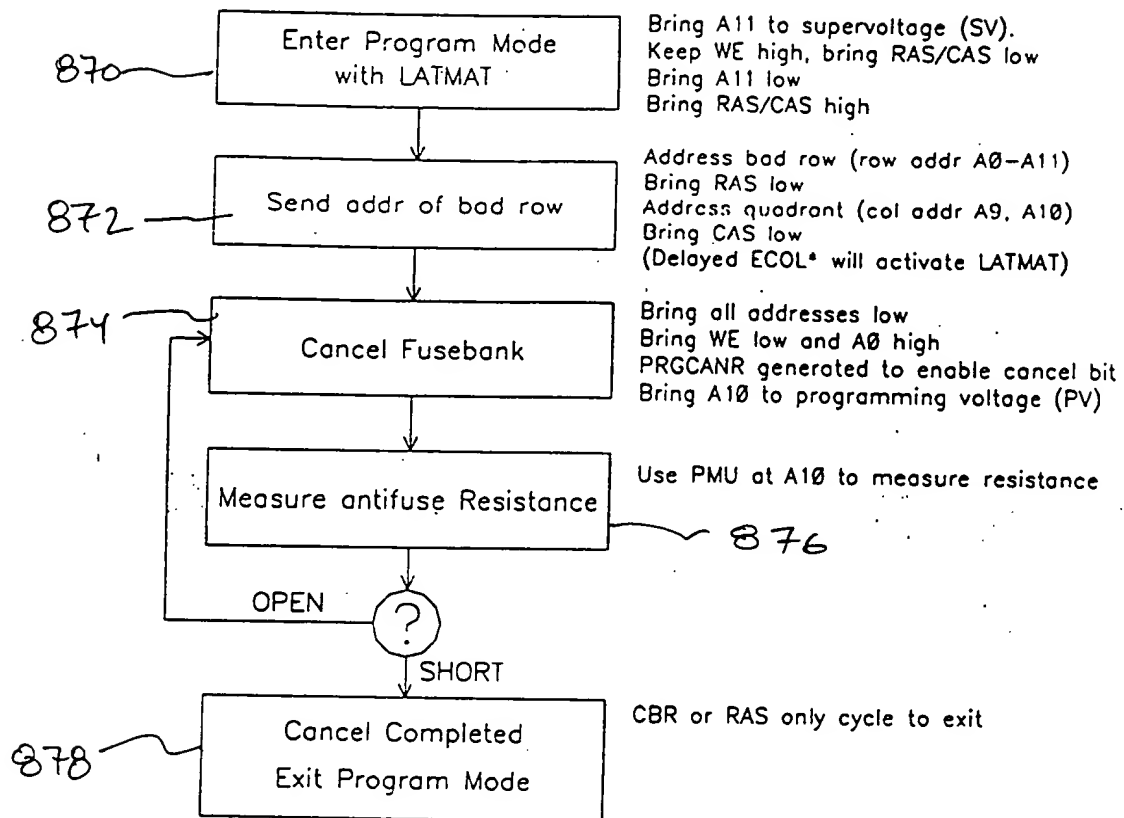


FIGURE 213



## Program Row Fusebank

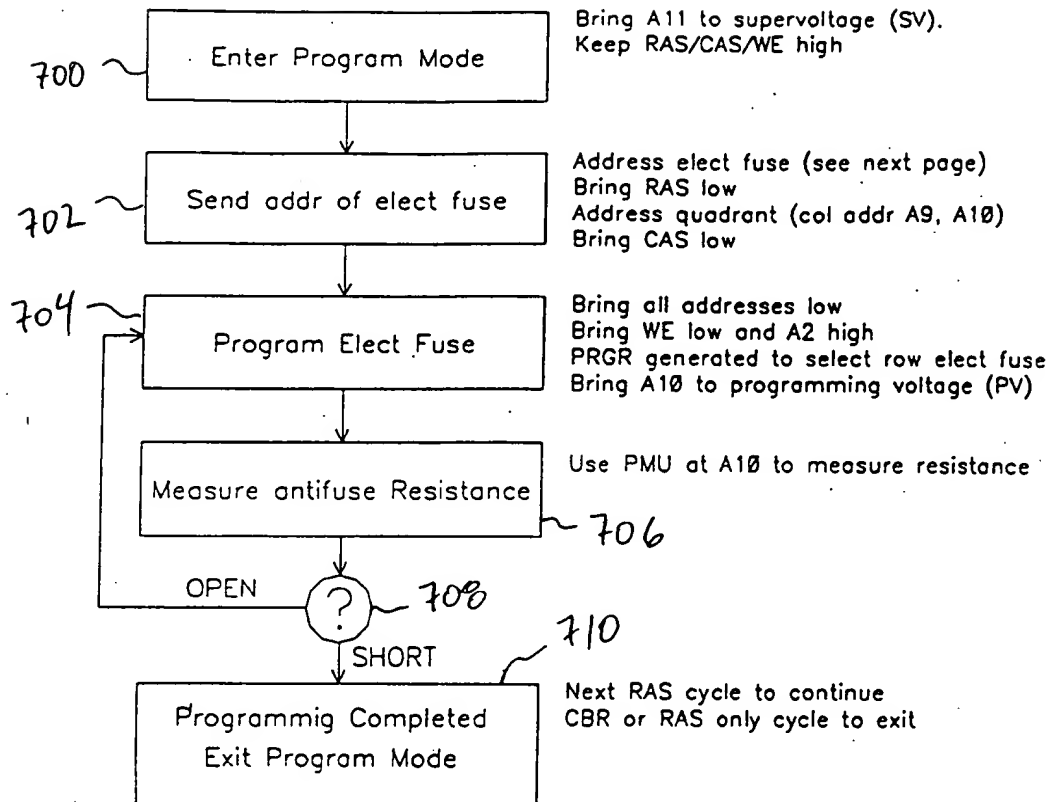


FIGURE 214

## Determine Need for Cancel

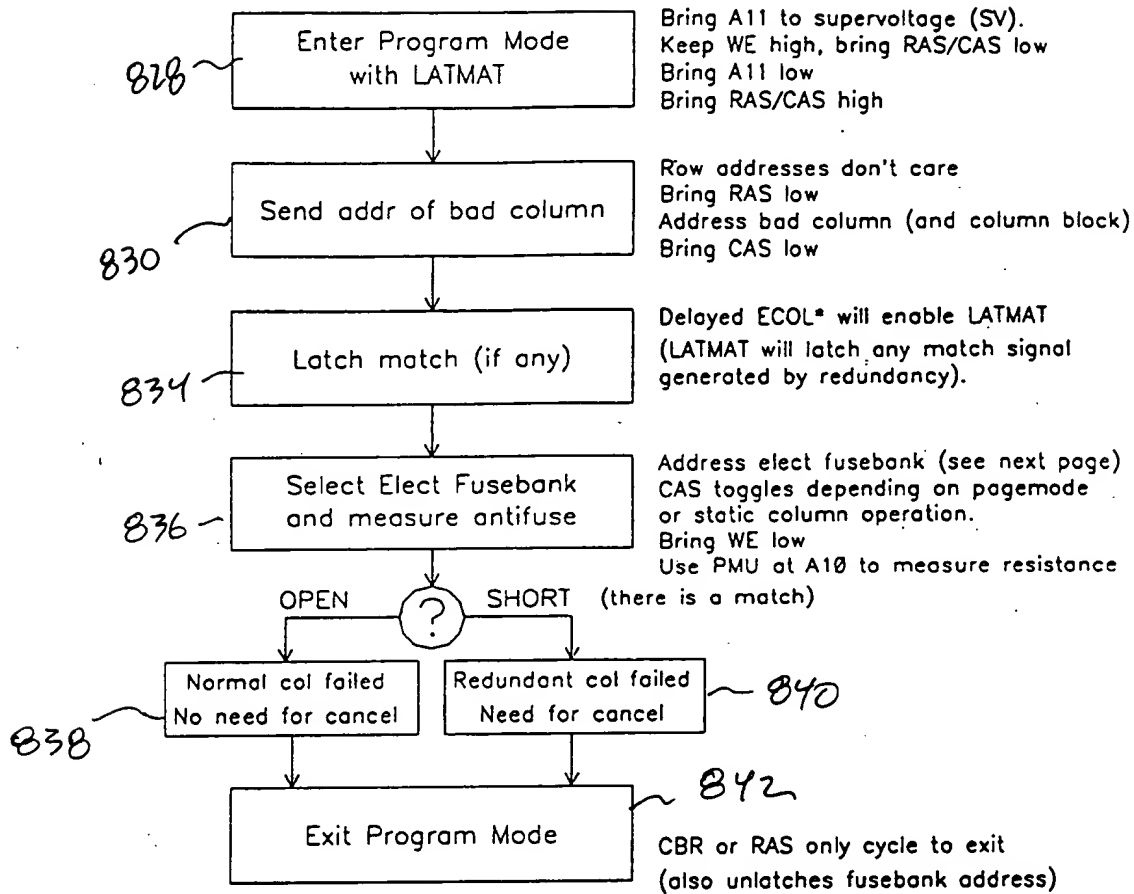


FIGURE 215

## Program Column Fusebank

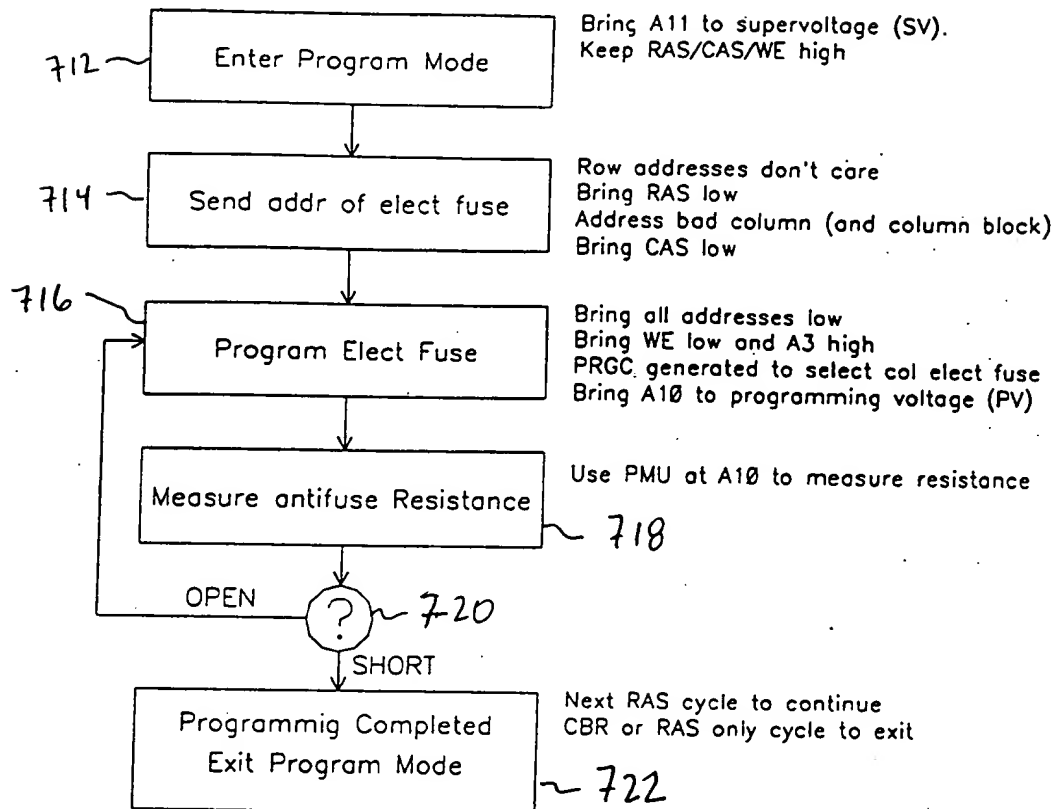


FIGURE 216

## Cancel Column Fusebank

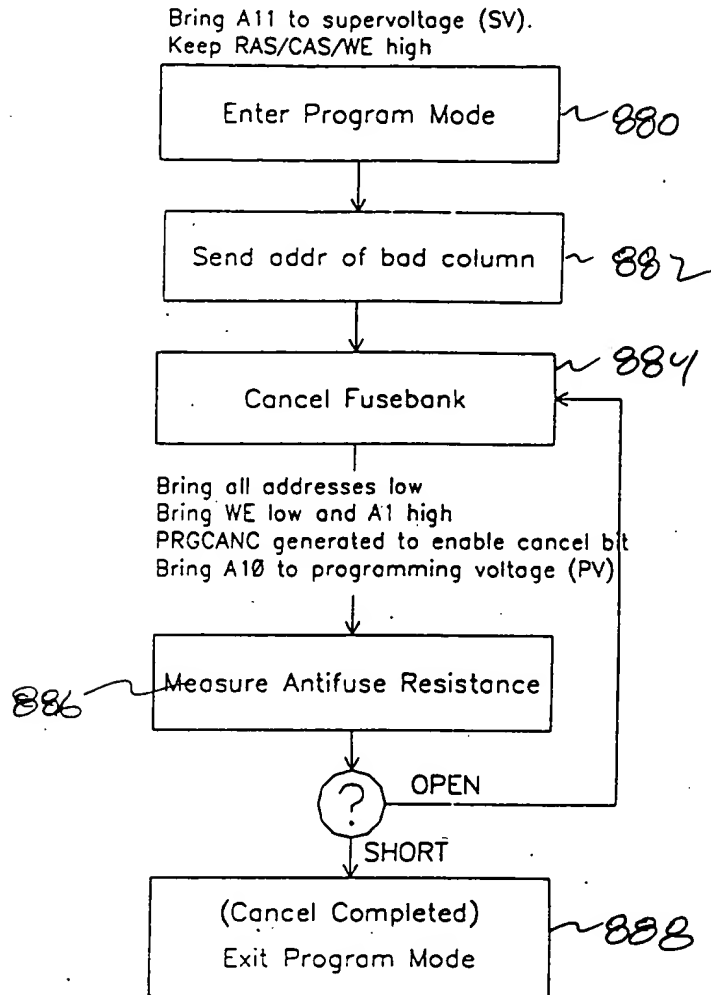


FIGURE 217

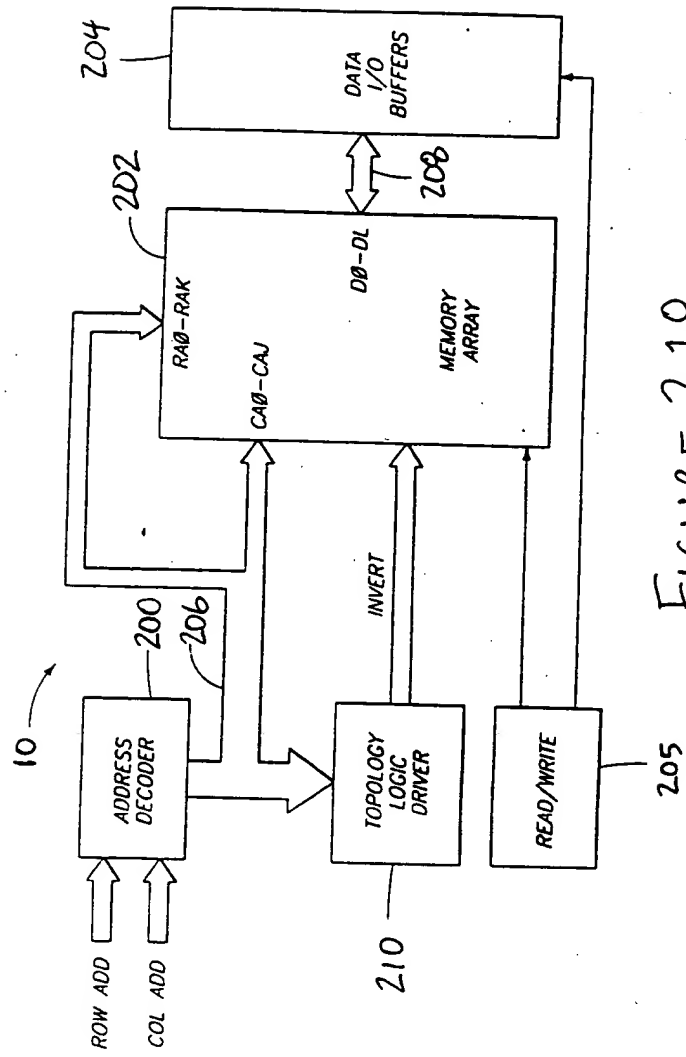
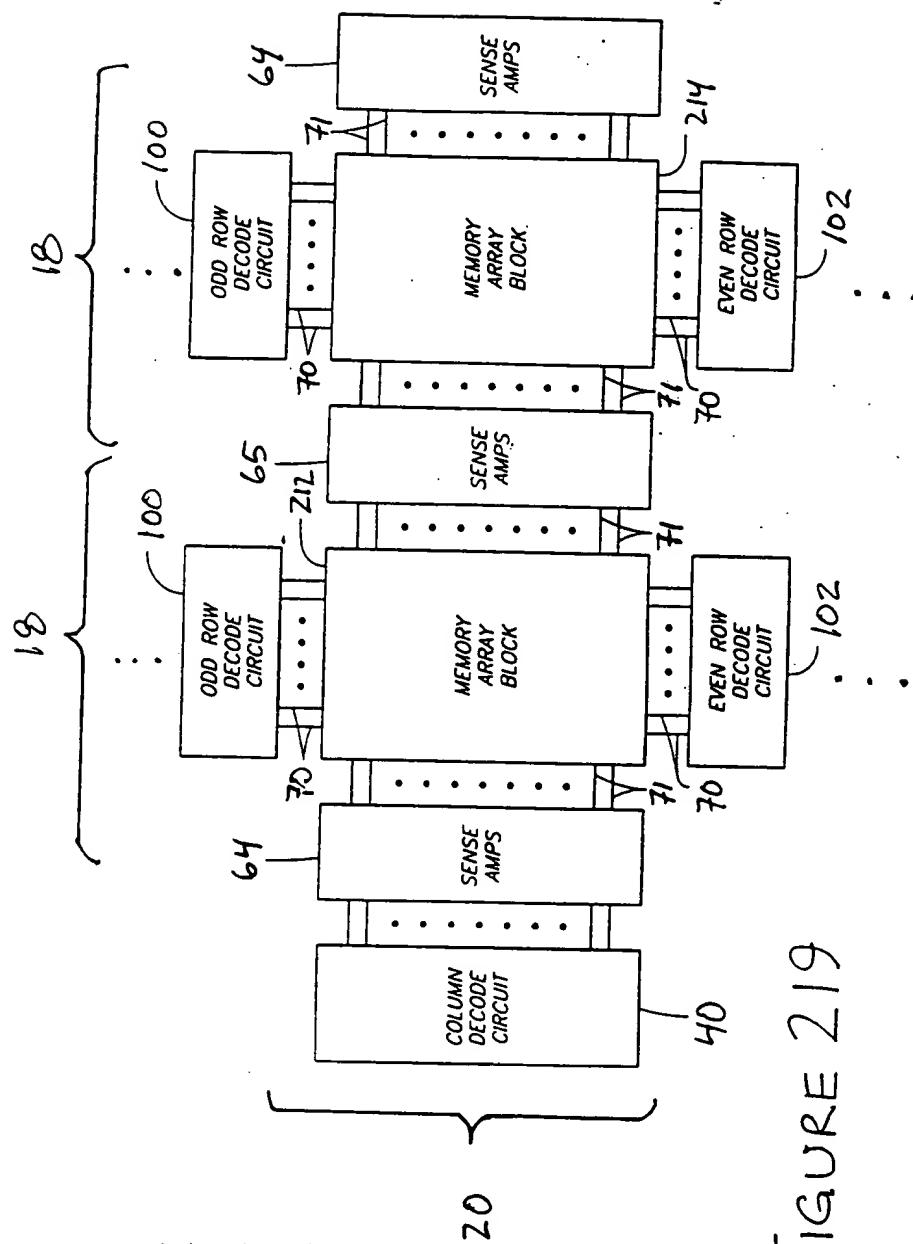


FIGURE 218



		TWIST				RA8=1			
		RA8=0							
RA0	RA1	RA8=0		RA8=1		RA8=0		RA8=1	
		R512	R513	R514	R515	R768	R769	R770	R771
0	0	1	0	1	1	0	1	0	1
0	0	0	1	1	1	0	0	1	1
CA2=0		D1 1	D0 1	D0 1	D1 1	D0 0	D1 1	D1 1	D0 0
		D0 0	D1 0	D1 0	D0 0	D1 0	D0 1	D0 1	D1 0
		D3 1	D2 1	D2 1	D3 1	D2 0	D3 1	D3 1	D2 0
		D2 0	D3 0	D3 0	D2 0	D3 0	D2 1	D2 1	D3 0
CA2=1		D3 0	D2 0	D2 0	D3 0	D2 1	D3 0	D3 0	D2 1
		D2 1	D3 1	D3 1	D2 1	D3 1	D2 0	D2 0	D3 1
		D1 0	D0 0	D0 0	D1 0	D0 1	D1 0	D1 0	D0 1
		D0 1	D1 1	D1 1	D0 1	D1 1	D0 0	D0 0	D1 1

FIGURE 22D

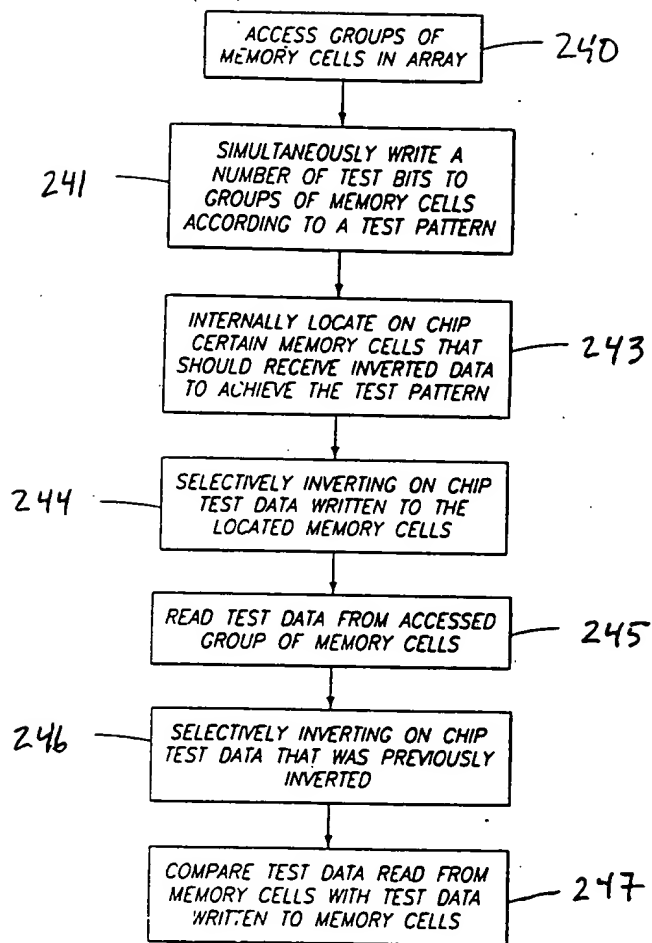


FIGURE 221



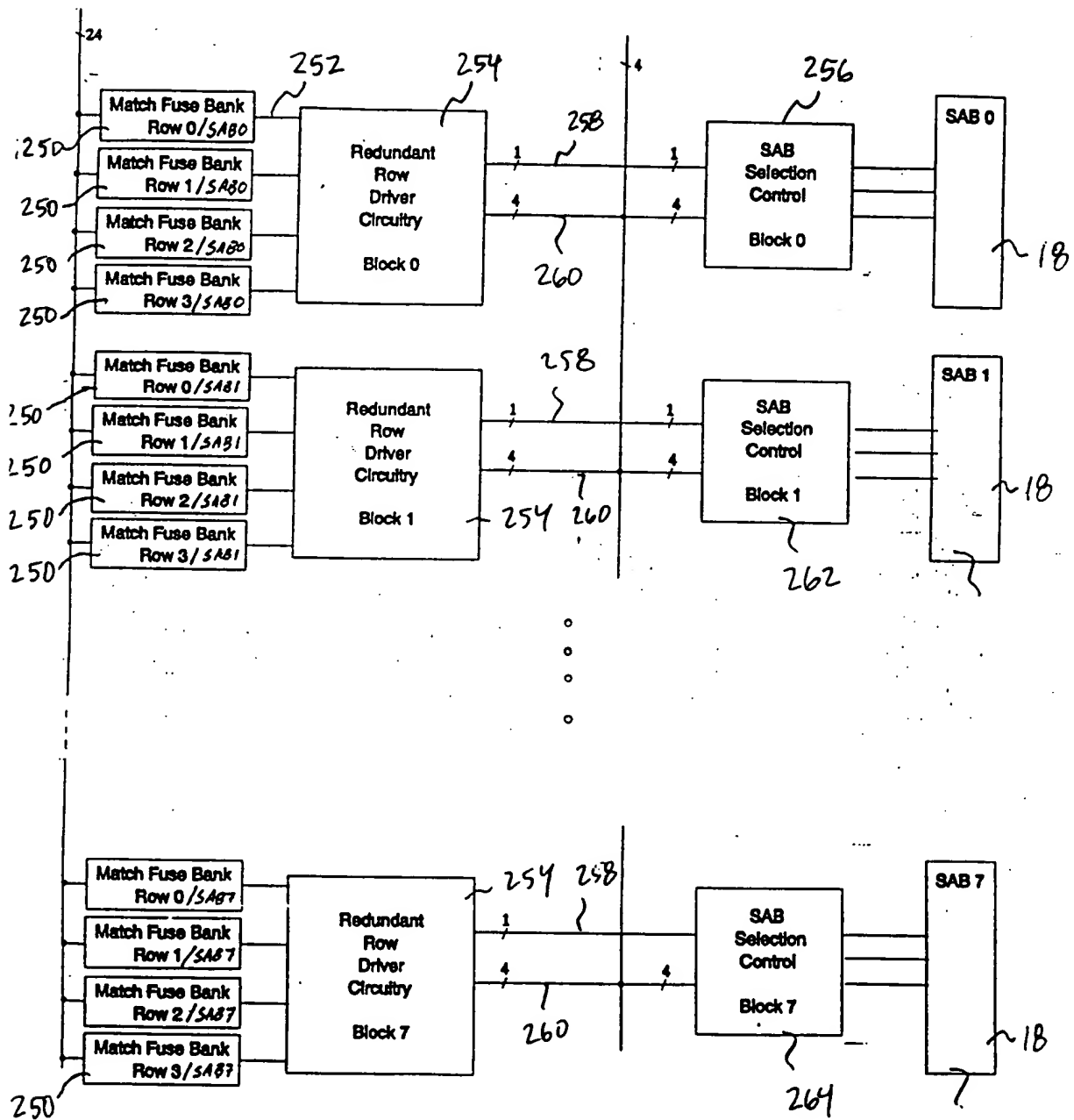


FIGURE 222

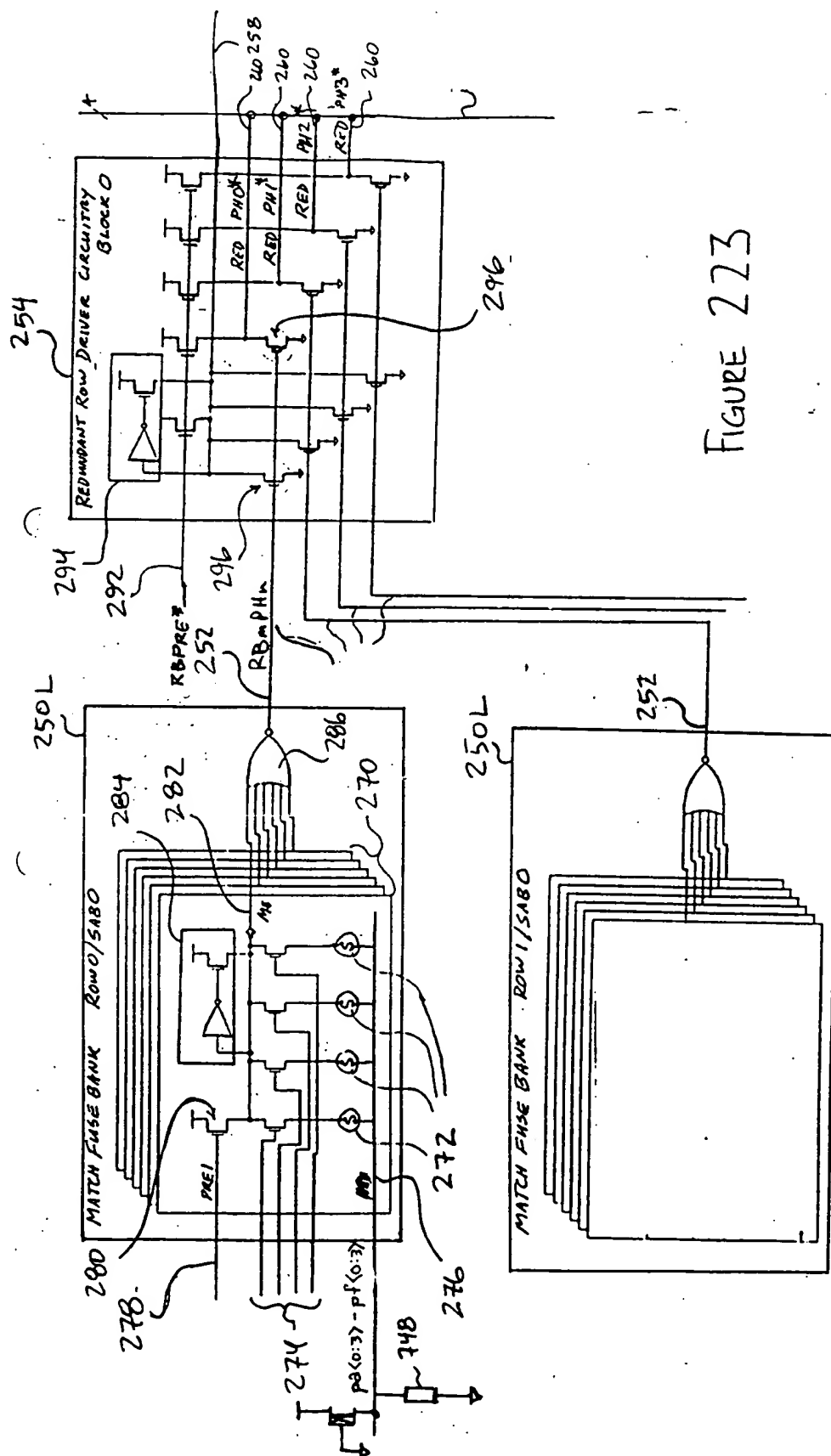


Figure 223

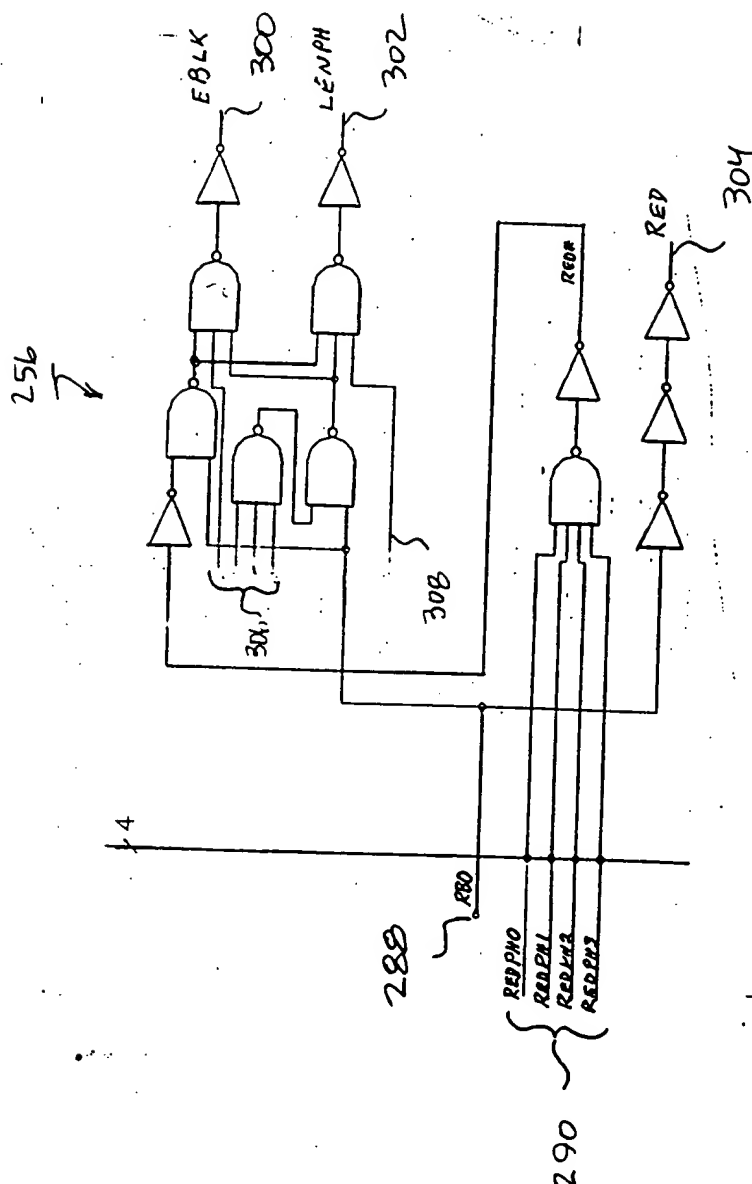


FIGURE 224

SAB0								
OPERATION TYPE			SELECTION CONTROL					
			Input			Output		
Primary Row to Fire ?	Redundant Row In SAB0 ?	Primary Address In SAB0 ?	Primary Address Lines	One of REDPH0-REDPH3	$\overline{RB0}$	EBLK	LENPH	RED
yes		yes	1	1	1	1	1	0
		no	0	1	1	0	0	0
no	yes	yes	1	0	0	1	1	1
		no	0	0	0	1	1	1
	no	yes	1	0	1	0	0	0
		no	0	0 or 1*	1	0	0	0

\* Depending on whether redundant row in another SAB is to fire

FIGURE 225

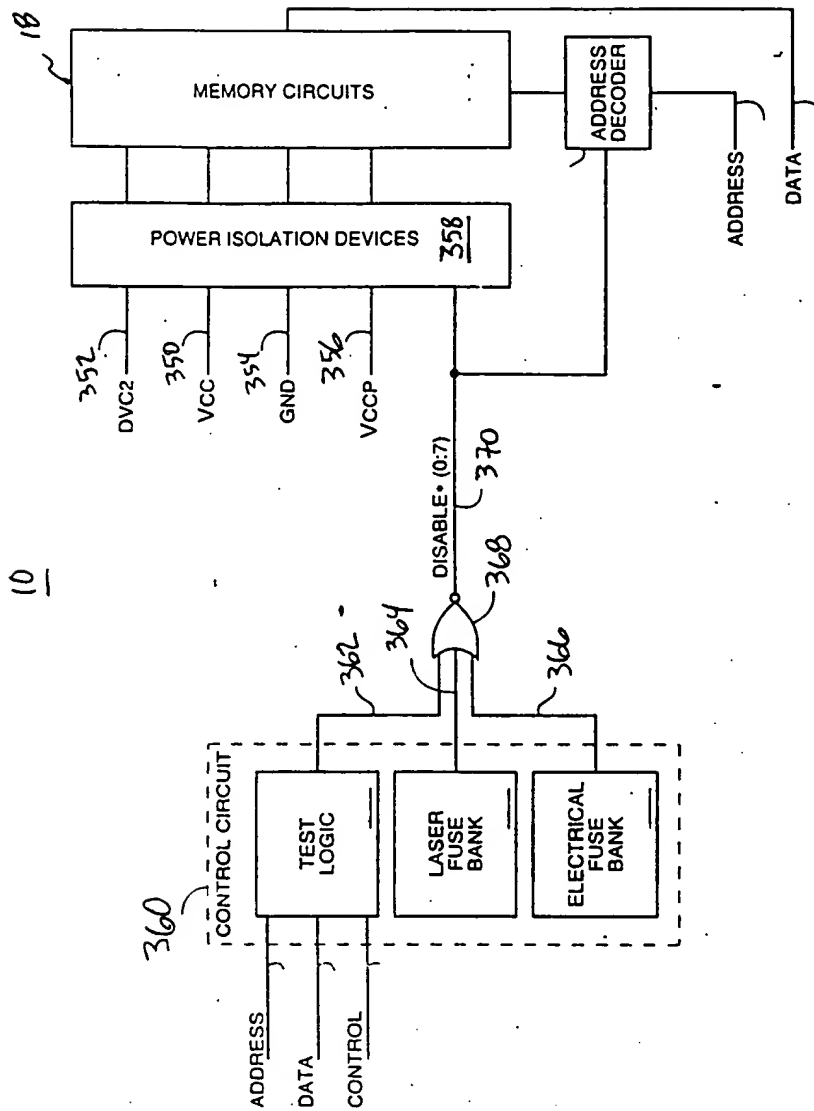


FIGURE 226

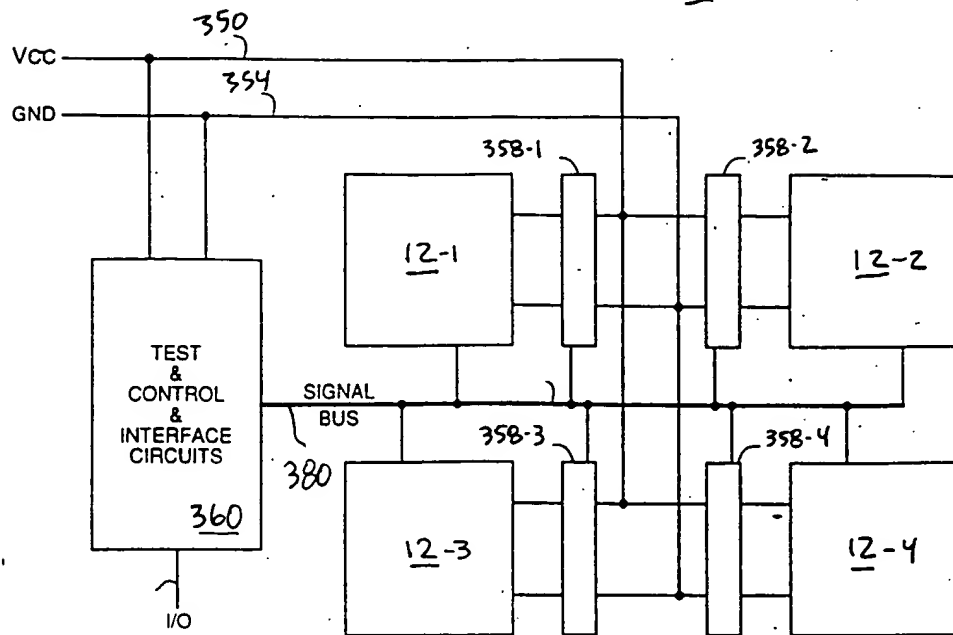


FIGURE 227

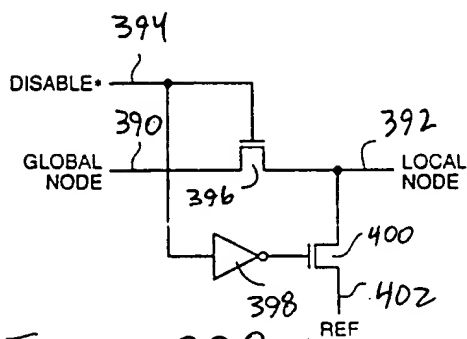


FIGURE 228

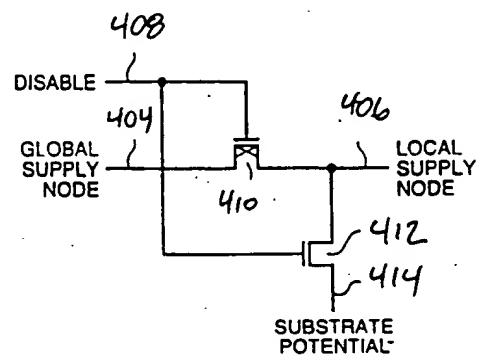


FIGURE 229

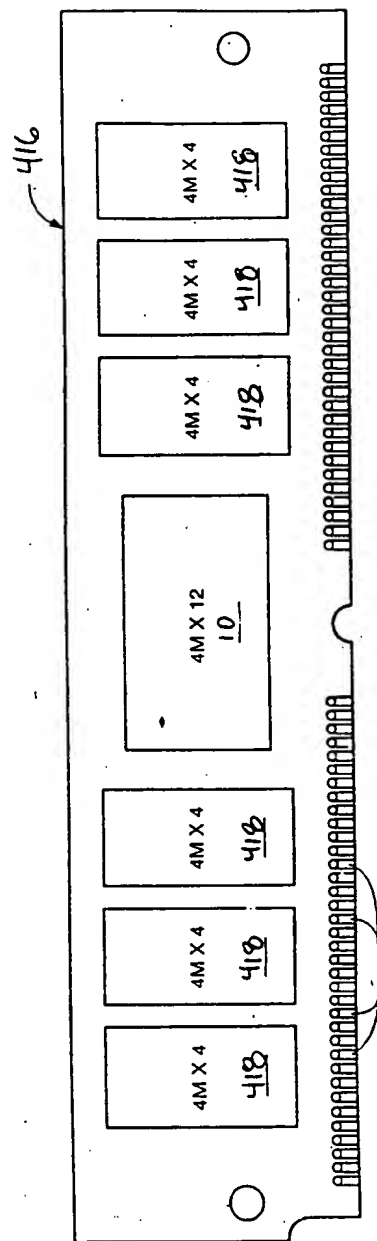


FIGURE 230

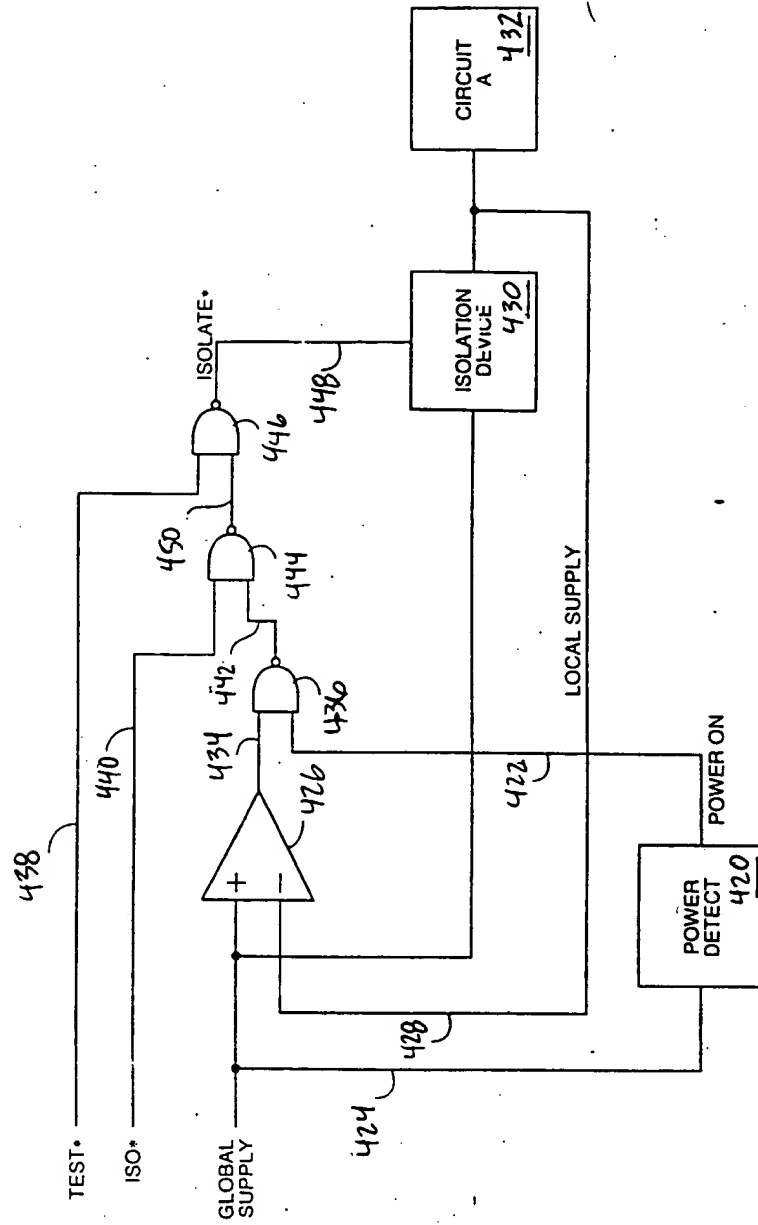


FIGURE 231



Anti-fuse not blown, Address=0

Anti-fuse blown, Address=1

Row Antifuse Selection Within Each Bank

Fuse Selection Address				Repair Address=1
A4	A3	A2	A1	
0	0	0	0	A1
0	0	0	1	A2
0	0	1	0	A3
0	0	1	1	A4
0	1	0	0	A5
0	1	0	1	A6
0	1	1	0	A7
0	1	1	1	A8
1	0	0	0	A9
1	0	0	1	A10
1	0	1	0	A0
1	0	1	1	A11
1	1	0	0	Enable Bank
1	1	0	1	—
1	1	1	0	—
1	1	1	1	—

FIGURE 232

# Row Fusebank Enable Selection

Row Fusebank	Fusebank Selection Address			
	A10	A9	A8	A7
R0	0	0	0	0
R1	0	0	0	1
R2	0	0	1	0
R3	0	0	1	1
R4	0	1	0	0
R5	0	1	0	1
R6	0	1	1	0
R7	0	1	1	1
R8	1	0	0	0
R9	1	0	0	1
R10	1	0	1	0
R11	1	0	1	1
R12	1	1	0	0
R13	1	1	0	1
R14	1	1	1	0
R15	1	1	1	1
LEFT	0	0		
RIGHT	0	1		

FIGURE 233

# Column Antifuse Selection Within Each Bank

Fuse Selection Address			Repair Address=1
A1	A0	A6	
0	0	1	A2
0	0	0	A3
0	1	1	A4
0	1	0	A5
1	0	1	A6
1	0	0	A7
1	1	0	A8
1	1	1	BANK ENABLE

FIGURE 234

# Column Fusebank Enable Selection

Column Fusebank	Fusebank Selection Address			
	A10	A9	A8	A7
C0	0	0	0	0
C1	0	0	0	1
C2	0	0	1	0
C3	0	0	1	1
C4	0	1	0	0
C5	0	1	0	1
C6	0	1	1	0
C7	0	1	1	1
C8	1	0	0	0
C9	1	0	0	1
C10	1	0	1	0
C11	1	0	1	1
C12	1	1	0	0
C13	1	1	0	1
C14	1	1	1	0
C15	1	1	1	1

FIGURE 235

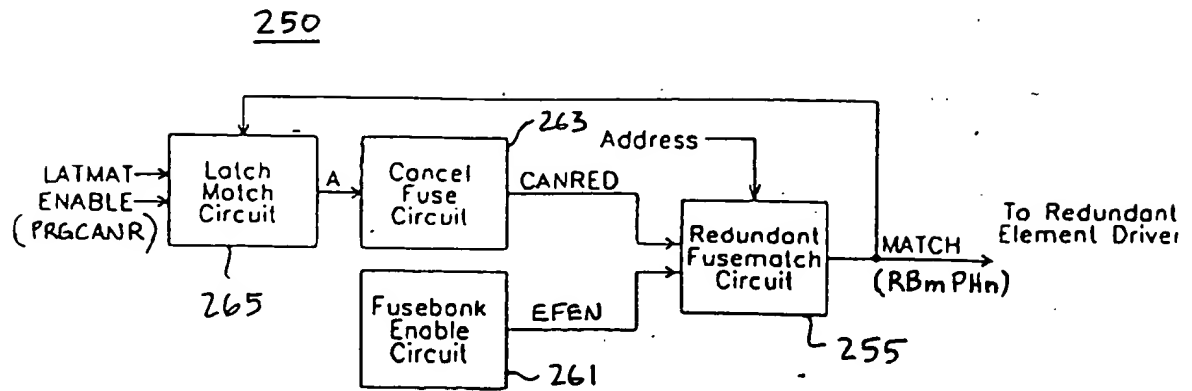


FIGURE 236

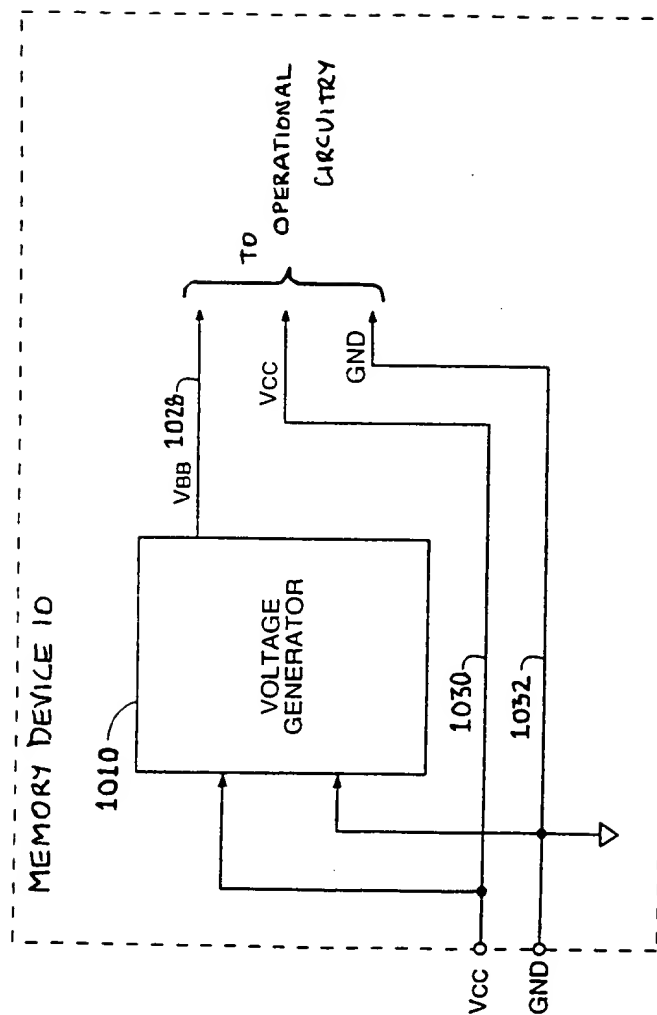


FIGURE 237

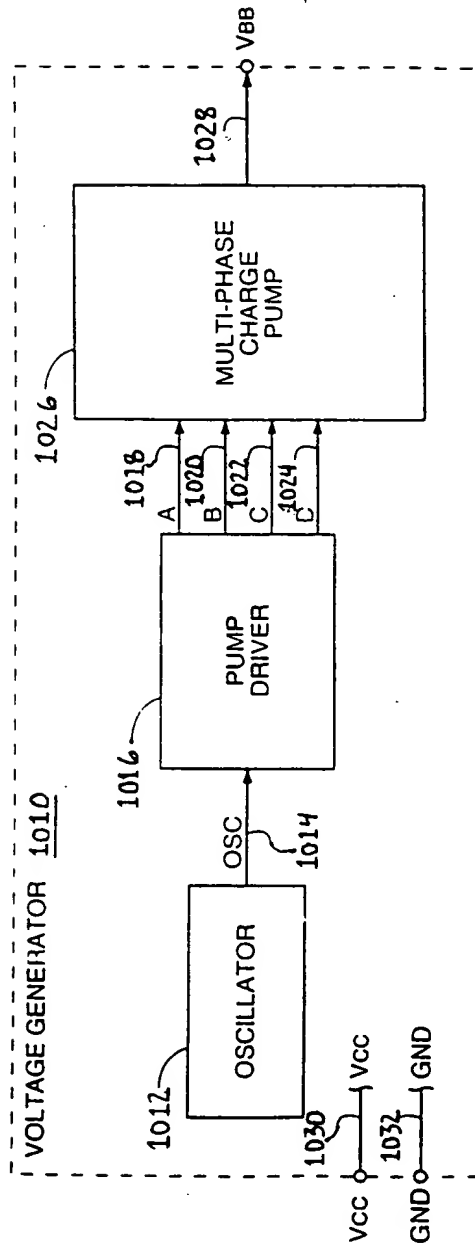


FIGURE 238

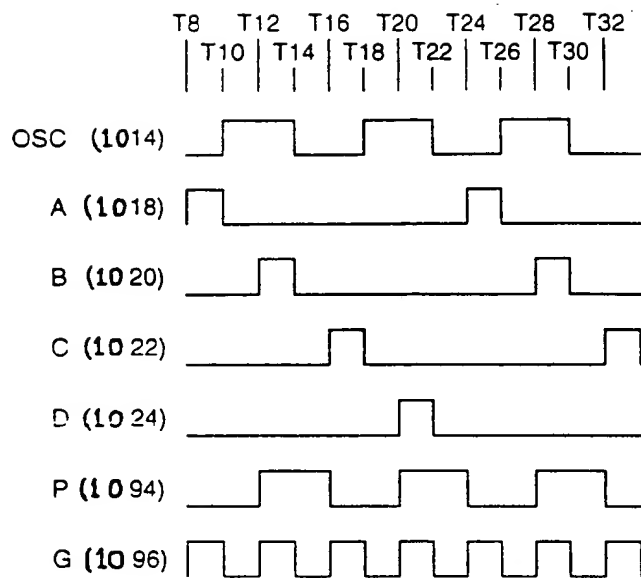


FIGURE 239



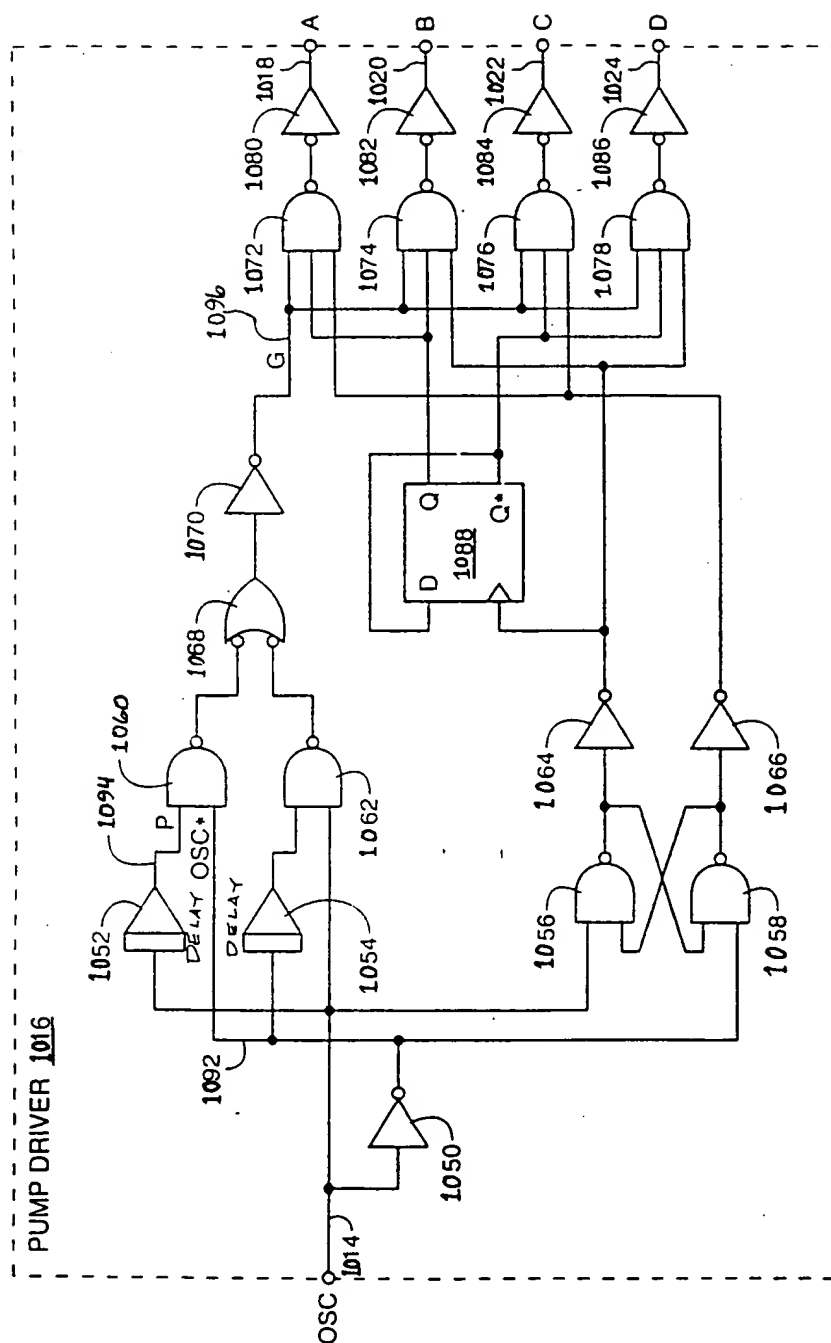


FIGURE 240

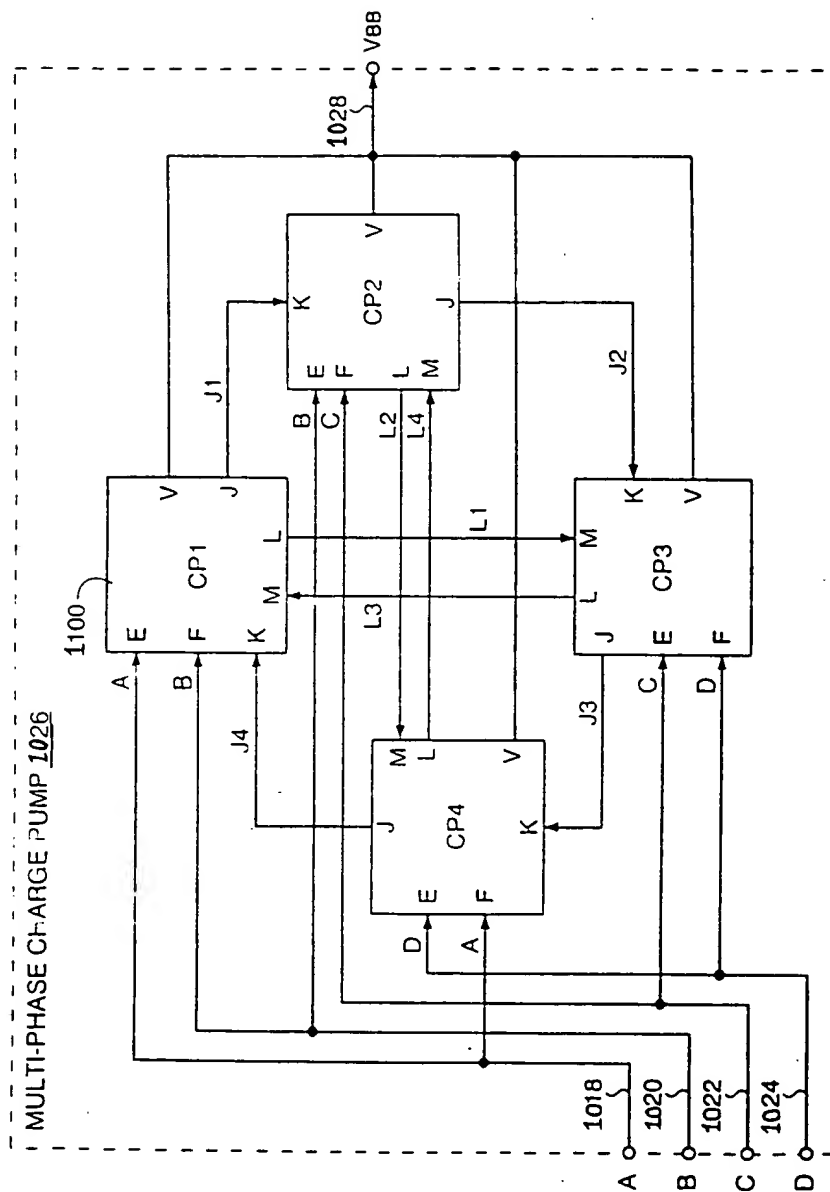


FIGURE 241

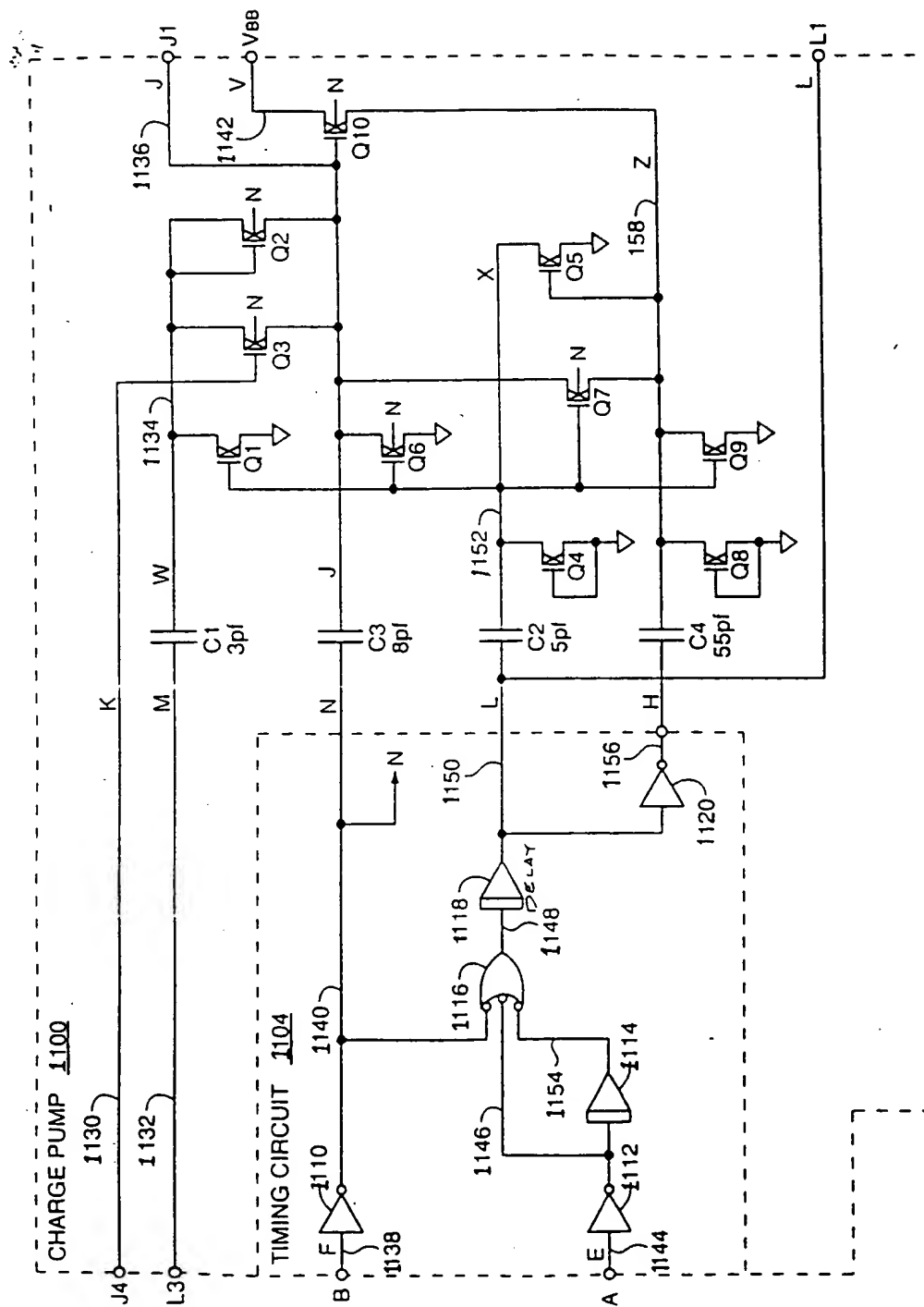


FIGURE 242

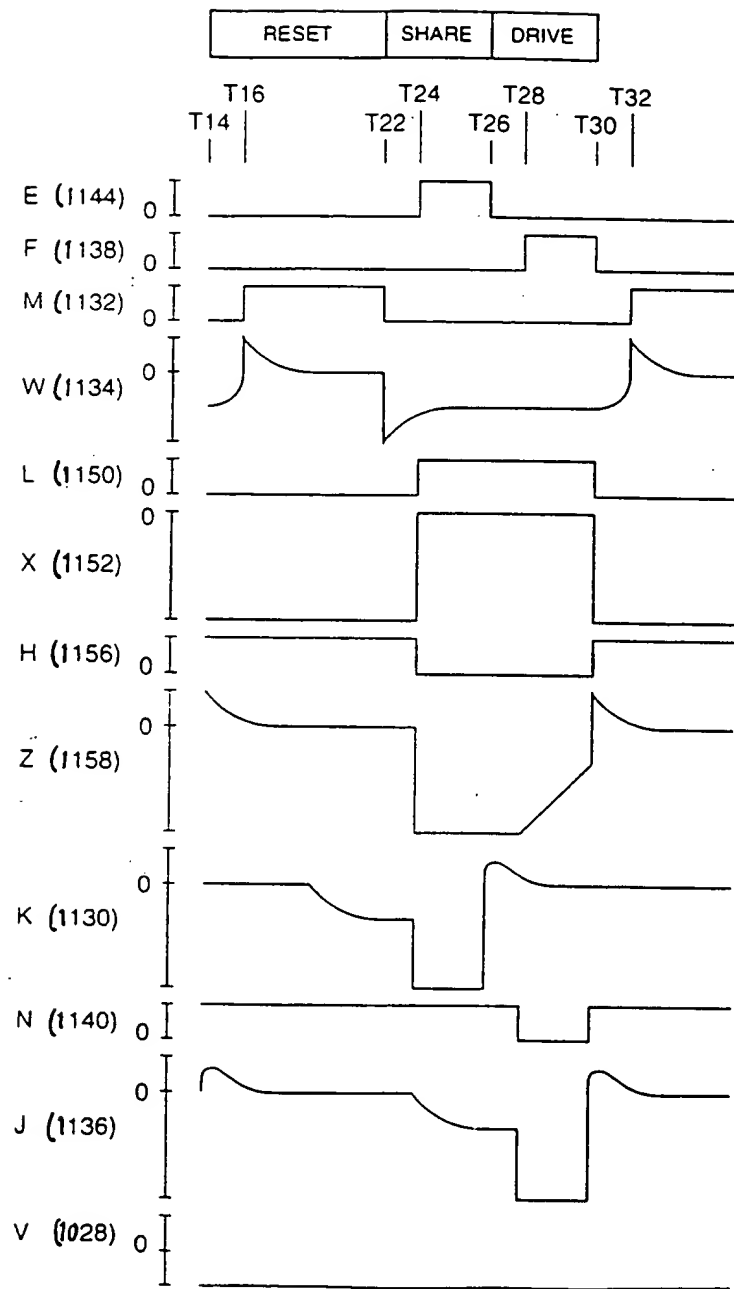


FIGURE 243

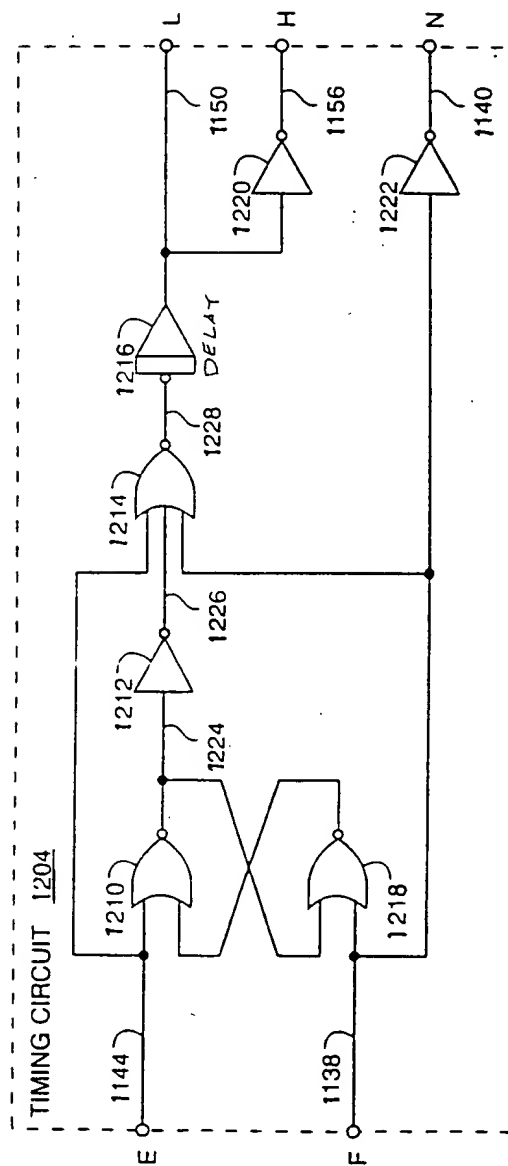


FIGURE 244

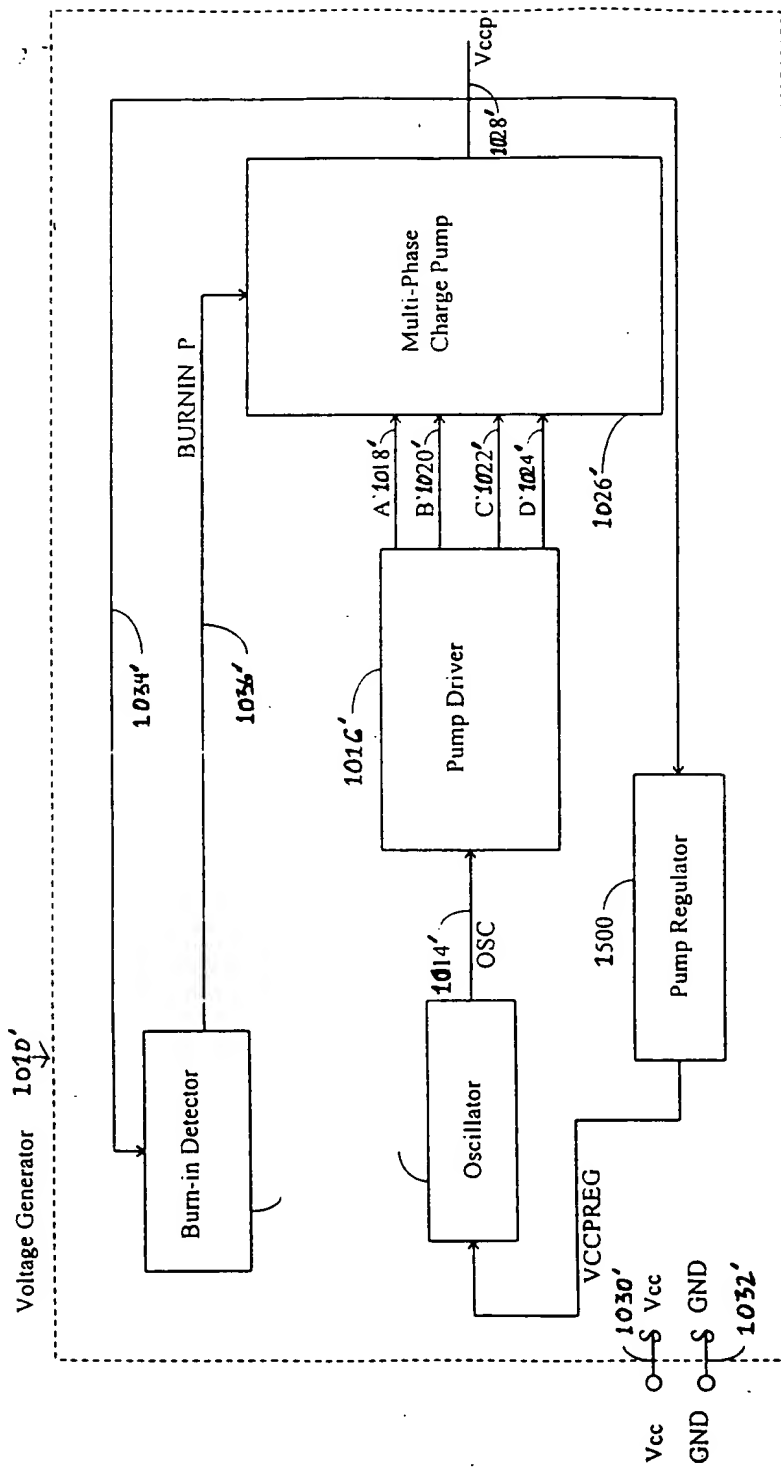


FIGURE 245

CHARGE PUMP 1300

V<sub>CC</sub> 1.030V

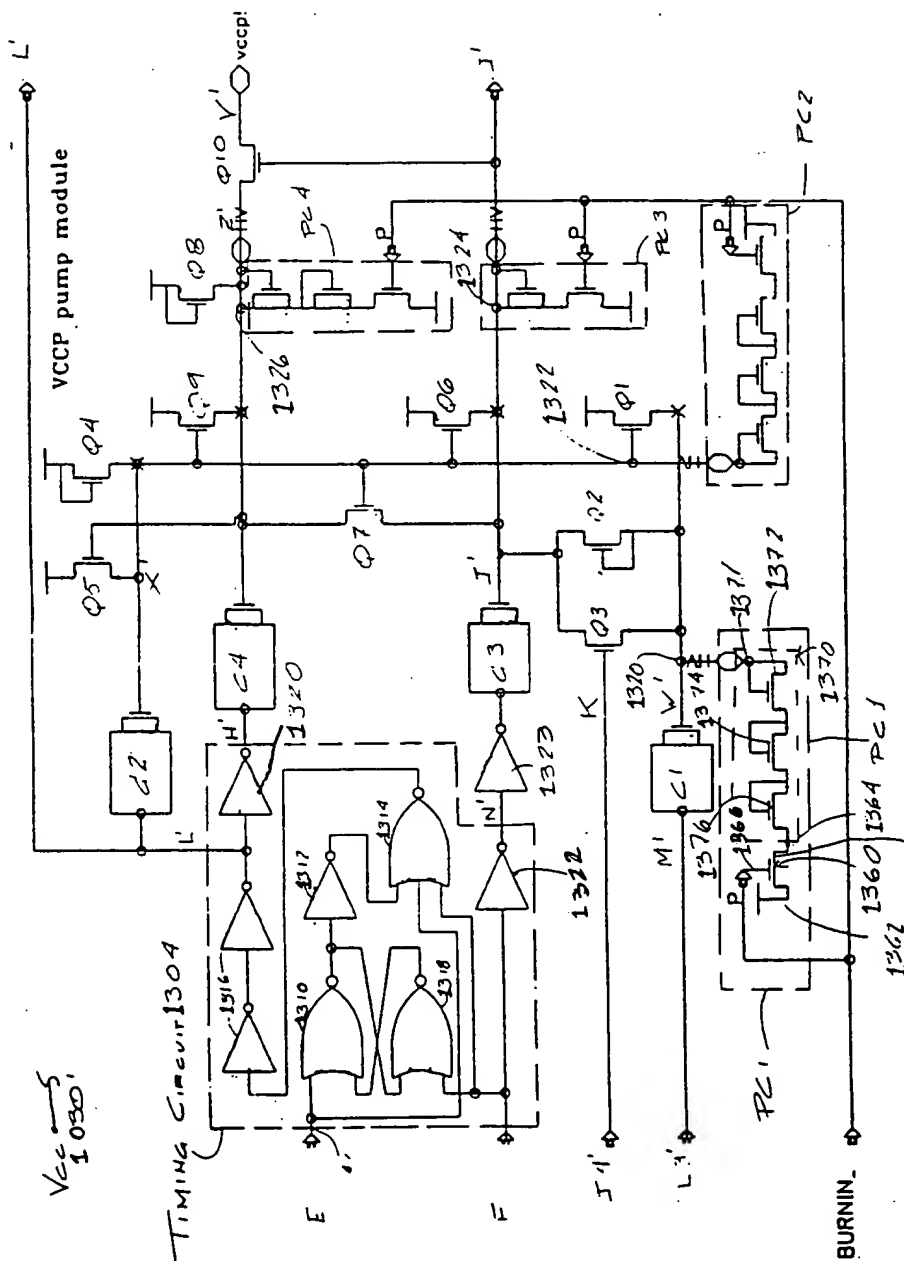


FIGURE 246

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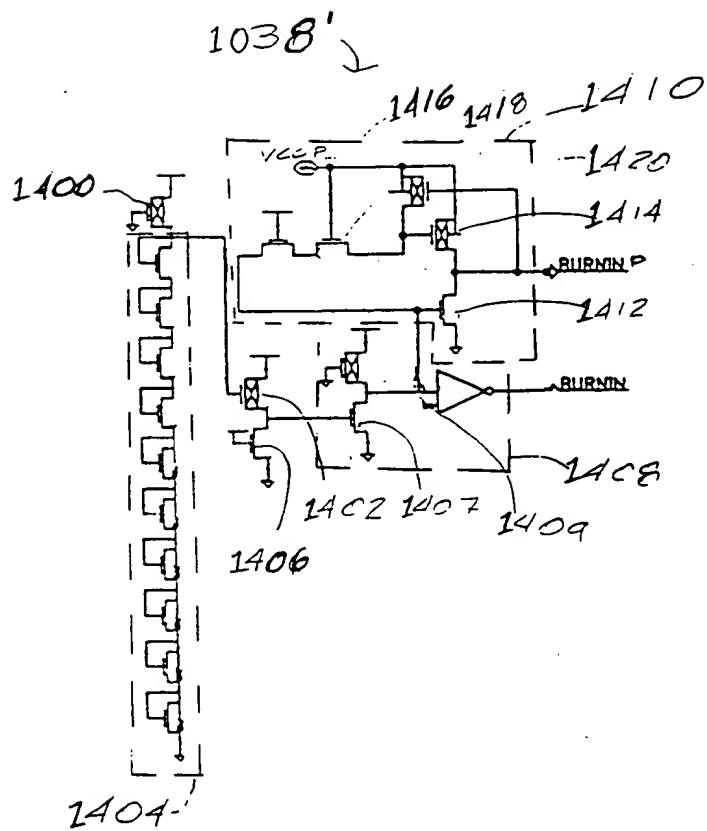


FIGURE 247



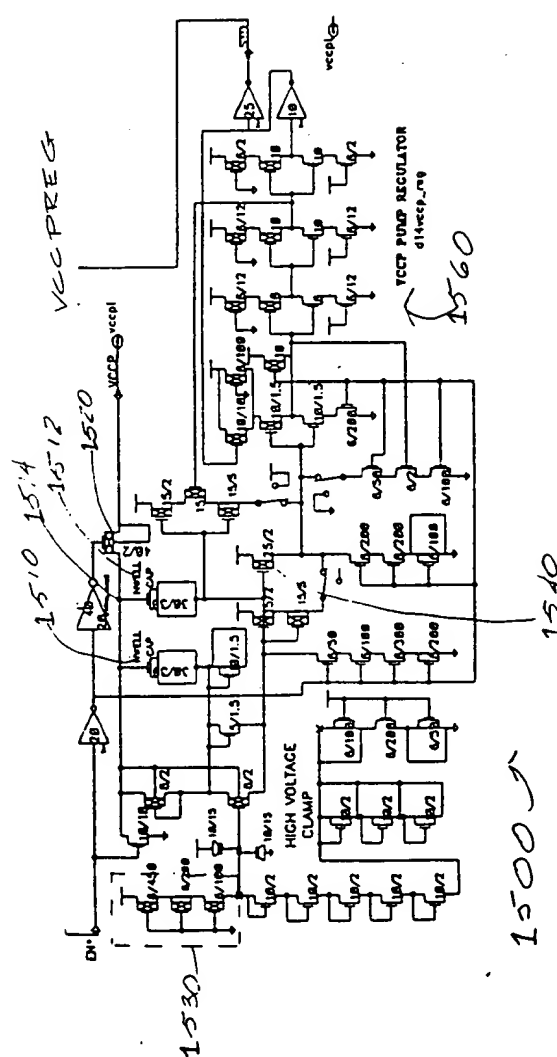


FIGURE 248